Plasma-assisted chemical vapor deposition of dielectric thin films for ULSI semiconductor circuits

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Plasma-assisted deposition of thin films is widely used in microelectronic circuit manufacturing. Materials deposited include conductors such as tungsten, copper, aluminum, transition-metal silicides, and refractory metals, semiconductors such as gallium arsenide, epitaxial and polycrystalline silicon, and dielectrics such as silicon oxide, silicon nitride, and silicon oxynitride. This paper reviews plasma-assisted chemical vapor deposition (CVD) applications and techniques for *dielectric* thin films. In particular, we focus on the integration, process, and reliability requirements for dielectric films used for isolation, passivation, barrier, and antireflective-coating applications in ultralarge-scale integrated (ULSI) semiconductor circuits. In addition, manufacturing issues and considerations for further work are discussed.

Introduction

The fact that a gas discharge containing charged (ion) and neutral (radical) species can be used to initiate chemical processes has been known for over a century [1]. In later studies, other material-transport phenomena using a high-frequency discharge with an applied external electrode had also been observed [1]. With regard to the latter, the first experimental result, by Anderson in 1962, showed that a radio frequency (rf) voltage can be applied inside a glass tube to create reactive species for thin-film deposition [2]. The following year, Atl et al. showed that this plasma-assisted CVD (or simply "plasma CVD") process could be used for microelectronic applications, especially for diffusion masks and passivation [3, 4]. However, the use of plasma-assisted deposition processes for microelectronic circuit manufacturing was not seriously considered until the introduction of commercial batch processing equipment in 1974 [5, 6]. Since then, plasma-assisted deposition processing has moved from research and

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development lines into current product manufacturing lines for integrated circuits (ICs). More research, development, and manufacturing applications of thin films formed by plasma deposition have appeared in the technical literature and various commercial products, especially for microelectronic devices, as discussed in many recent publications [7–11].

In recent years, new materials requirements and lower-processing-temperature requirements in ULSI circuits, solar energy cells, flat-panel displays, and optical systems have made plasma-assisted deposition processes increasingly important. In general, films of silicon-based semiconductors and insulators such as boron-doped or phosphorus-doped and intrinsic amorphous silicon, silicon oxide, phosphorus-doped and/or boron-doped silicon oxide, silicon nitride, and silicon oxynitride deposited by plasma-assisted CVD are most frequently used in solar energy cells [12], xerography [13], thin-film transistors for active-matrix liquid crystal displays [14–16], and ICs. There are many reviews of plasma deposition processes [17–19], relevant theory and reaction mechanisms [17, 20, 21], critical issues and parameters [22], and applications in IC fabrication [7–11, 22–24].

Current requirements for ULSI applications

Five principal types of silicon-based thermal and plasma CVD dielectrics are currently used in IC fabrication: silicon oxide, silicon nitride, silicon oxynitride, phosphorus-doped silicon oxide (PSG), and boron/phosphorus-doped silicon oxide (BPSG). Their properties can be modified to achieve desirable functions. For example, silicon-rich silicon oxide or nitride films can be used as charge-storage materials for erasable programmable read-only memory (EPROM) devices. The composition of silicon oxynitride can be tailored to meet specific photolithography and etching (or simply "etch") requirements as an antireflective coating (ARC) [25] and also to meet device and integration requirements as a barrier film for gate conductors (to be described later). The gap-filling (or simply "gap-fill") capability and degree of local planarization for high-density plasma (HDP) CVD oxide [26] can be adjusted by changing the deposition-to-sputter-etching ratio (or simply "sputter-etch ratio") D/S, defined as (net deposition rate + blanket sputtering rate)/(blanket sputtering rate). The requirements change for HDP CVD oxide when considering it for use in shallow-trench isolation (STI) compared to use as an intermetal dielectric (IMD). For example, maintaining a wafer temperature less than 400°C is critical for the IMD application for better metal reliability [27]. A higher temperature is desirable for the STI application, since a more dense film that is highly resistant to subsequent wet-etching steps is thus obtained. These applications are discussed in more detail later in the paper.

One of the major requirements and technology drivers for ULSI isolation and passivation dielectrics is the filling of sub-half-micron-wide gaps without voids. The film profile changes with the type of deposition process used. For conventional plasma-enhanced (PE) CVD processing, the deposited dielectric film takes on a "bread-loaf" profile, as illustrated in **Figure 1**. This type of profile is most pronounced with silane-based PECVD films. When tetraethylorthosilicate (TEOS) is used as the silicon source for PECVD oxide deposition, there is less cusping because of the higher surface mobility of the reactants [28]; however, a void still forms if the gap is small enough, because the conformality of the film is not 100%. This means that the amount of deposition on the sidewalls and bottom of the trench portion of a feature is less than on the top of the feature. So, in order to use PECVD films alone for gap-fill applications, they are typically used in conjunction with an argon sputter etch in a multistep PECVD–argon sputter etch–PECVD sequence described previously [29]. Conformal deposition is more typical for thermal (non-plasma) CVD processes such as low-pressure (LP) CVD at high temperatures or for ozone–TEOS atmospheric or subatmospheric pressure (AP or SA) CVD at lower temperatures (less than 600°C). Furthermore, HDP CVD results in a completely different type of profile, as indicated in Figure 1, because of the "bottom-up" deposition from the simultaneous deposition and etching. The resultant topography from any of these CVD processes plays a decisive role in the choice of subsequent planarization techniques.

Typically, thermal CVD processes such as LPCVD BPSG, APCVD (or SACVD) BPSG, or PSG are used to passivate the polysilicon/metal silicide gate conductor for sub-half-micron devices because of their high-aspect-ratio[1] fill capability compared to plasma CVD processes and because there are no plasma damage concerns with thermal CVD processing. Process-induced IC device damage from plasma processing (in particular at the gate-conductor level, because there is no device protection) is a critical issue for the PECVD passivation dielectrics. Our work on PECVD PSG plasma damage has been published in detail elsewhere [29–33]. Briefly, low process pressure during deposition of the PECVD PSG was identified as the main factor causing gate-oxide charge damage. Increasing the pressure for the PECVD PSG process regardless of dopant source (trimethylphosphite or triethylphosphate) resulted in no charge damage on antenna test sites and device structures. A more recent study describes another technique used to optimize a PECVD PSG process for plasma damage designated as corona oxide semiconductor (COS) charge measurement [34]. The technique, combined with the antenna test

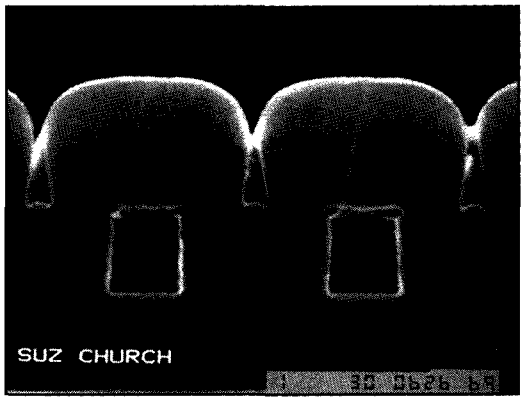
[1] Aspect ratio is defined as the height of the line divided by the width of the trench.

structure method of measuring plasma damage, provides a fast and cost-effective way to optimize plasma CVD processes.

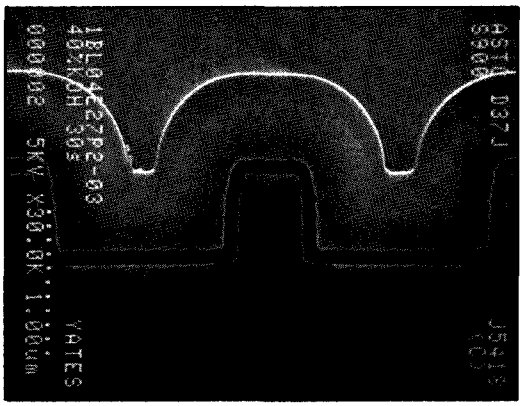
Doped silicon oxide films such as PSG or BPSG are preferred for gate-conductor passivation because of their mobile ion barrier properties [35, 36], low reflow temperature for local planarization (applies to BPSG only), high etch selectivity to the underlying barrier layer (e.g., nitride [37]), and faster polishing rate compared to undoped silicon oxide. In this paper, we discuss our recent work with HDP CVD PSG including gap-fill and plasma damage results. We have previously published an overview of our own work and that of others in IBM on relevant thermal CVD processes and applications [29].

The gap-fill requirement for dielectrics in the "back-end-of-line" (BEOL) depends on the interconnect fabrication methods used. Multilevel interconnects usually involve two types of planarization methods: the planarization of interlayer dielectrics and the planarization of metal layers. For the former, for example, an Al(Cu)-based layer is patterned into lines and the insulator is deposited between the spaces and above the lines. Therefore, a critical requirement in this case is the filling of the gaps between the lines without void formation. Void-free filling of high-aspect-ratio features is not a simple matter and requires the use of advanced insulator deposition processes such as HDP CVD. For submicron metal interconnect fabrication, the insulator deposition is generally followed by partial planarization using spin-on-glass (SOG) [38–40], a resist etch-back [38, 41–43], or a global planarization using, for example, chemical–mechanical polishing (CMP). For the planarization of metal layers, the damascene technique is most commonly used; several papers reporting its use in IBM have been published [44–47]. Using this technique, a dielectric such as silicon oxide is deposited on a planar surface and the wiring level is patterned into the dielectric using photolithography and RIE. A thin metal liner and a metal such as tungsten (or aluminum or copper) are then deposited on the patterned dielectric and subsequently planarized by CMP, stopping on the dielectric and leaving metal in the patterned features. Therefore, in the damascene technique, the metal rather than the insulator must fill the high-aspect-ratio features.

A critical film parameter for both interconnect fabrication techniques is the dielectric constant (k) of the IMD material. Use of a material having a lower dielectric constant leads to lower total capacitance, decreasing the interconnection delay and power dissipation [48], and thus enhancing performance. To achieve long-range interconnection performance objectives, low-dielectric-constant IMD will be required [49]. The dielectric constant of PECVD silicon oxide is typically 4.1–4.2. By doping the oxide with



(a)



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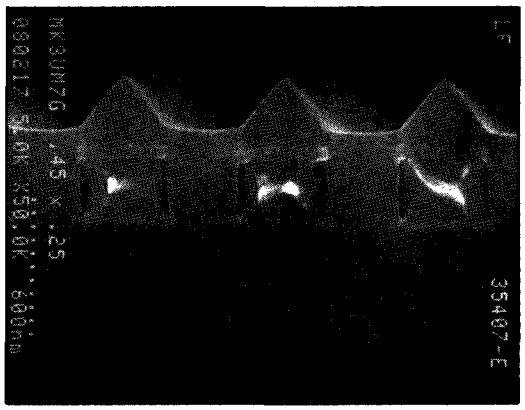


(c)

Figure 1

Scanning electron micrographs of cross sections of films deposited by (a) PECVD, (b) SACVD, and (c) HDP CVD. Note that TEOS was the silicon source for the PECVD and the SACVD, and silane for HDP CVD. The typical "bread-loaf" profile of the PECVD oxide film can be adjusted by varying process parameters such as temperature, pressure, and silicon source. The profile of the SACVD oxide film is conformal, and the unique profile of the HDP CVD oxide film is a result of simultaneous etching and deposition. Note that SACVD is a non-plasma process.

Table 1 Typical electron-impact reactions of silane molecules in an rf plasma discharge. The asterisk (*) refers to electronic excited state. From [1].

Reactant	*Reaction products*	*Enthalpy of formation* (eV)
$e^- + SiH_4 \rightarrow$	$SiH_2 + H_2 + e^-$	2.2
	$SiH_3 + H + e^-$	4.0
	$Si + 2H_2 + e^-$	4.2
	$SiH + H_2 + H + e^-$	5.7
	$SiH^* + H_2 + H + e^-$	8.9
	$Si^* + 2H_2 + e^-$	9.5
	$SiH_2 + 2H_2 + 2e^-$	11.9
	$SiH_3 + H + 2e^-$	12.3
	$Si^+ + 2H_2 + 2e^-$	13.6
	$SiH^+ + H_2 + H + 2e^-$	15.3

Table 2 Initial electron-impact reactions. From [1].

Excitation (rotational, vibrational, and electronic)	$e^- + A_2 \rightarrow A_2^* + e^-$
Dissociative attachment	$e^- + A_2 \rightarrow A^- + A^+ + e^-$
Dissociation	$e^- + A_2 \rightarrow 2A\cdot + e^-$
Ionization	$e^- + A_2 \rightarrow A_2^+ + 2e^-$
Dissociative ionization	$e^- + A_2 \rightarrow A^+ + A + 2e^-$

fluorine, the dielectric constant can be reduced to 3.0–3.7, depending on the fluorine concentration [50]. Si–F replaces the Si–OH and Si–H bonds in the oxide; since fluorine is more electronegative, the polarization changes, lowering the dielectric constant. SOG dielectrics (siloxanes, silsesquioxanes) and organic polymers formed by spin coating (polyimides, fluorinated polyimides, bisbenzocyclobutenes), poly(arylethers), or vapor-phase deposition (parylene N, parylene F, teflon) provide dielectric constants in the range of 1.9–3.0 [51]. Most polymers with a dielectric constant less than 3 are stable to only about 350°C. However, a recent publication on laser-evaporated siloxane thin films reports a dielectric constant of 2.0 and thermal stability to 400°C, although integration results were not published [52]. Also, it has been reported that parylene exhibits a high thermal stability [53], and its successful integration into a metal RIE BEOL has been demonstrated [54]. However, damascene integration may be more difficult to achieve because of the softness of parylene films. Spun-on films of materials such as nanoporous silica and xerogels exhibit a higher thermal stability and low dielectric constants (1.3–2.5), depending on their porosity [55–57], but associated process integration is challenging. There has been increased development activity in plasma-assisted CVD of amorphous carbon and fluorinated carbon films because of their low dielectric constants (2.3–2.7) and thermal stability up to 400°C [58–63]. Relevant work on insulators having low dielectric constants has been described elsewhere [48, 64–66].

In this paper, we discuss the plasma-assisted CVD of low-dielectric-constant insulators of potential interest at the ULSI level, including fluorine-doped silicon oxide and amorphous carbon and fluorocarbon. For related discussions, see the papers by Grill [67] and Nguyen [26] in this issue. To be suitable for the deposition of such insulators, plasma-assisted CVD should be applicable at relatively low substrate temperatures, should not damage underlying layers or devices that may be present on the substrate during deposition, and should produce insulators which, in addition to having low dielectric constants, satisfy etching, annealing, planarization, and stability requirements.

Fundamentals of plasma CVD

For microelectronics applications, the plasma CVD processes of interest are conventional PECVD, remote PECVD, and HDP CVD. We focus on conventional PECVD processing and describe HDP CVD processing briefly, since a more comprehensive paper by S. Nguyen [26] in this issue reviews that process. A recent review by Lucovsky [68] covers the evolution of low-temperature remote plasma-assisted deposition for device-quality silicon oxide and silicon nitride thin films. Briefly, remote PECVD differs from conventional PECVD in that the substrate is not in direct contact with the plasma and thus is not subjected to ion bombardment; also, process gases and diluents can be introduced either into the plasma region or downstream from the plasma. These differences have important effects on the final quality of the deposited films and the associated silicon–silicon oxide interface, and are key to forming device-quality dielectrics. Device-quality dielectrics have been deposited using other plasma processes such as He–PECVD [69], developed at IBM. The process produces high-quality insulators. It utilizes relatively high levels of helium dilution of the reactant gases, minimizing the amount of process-induced surface damage. The reader is referred to the aforementioned papers and references therein for details on device-quality dielectrics.

In thermal CVD, gas-phase reactive species are generated by heating of initial reactants. In plasma CVD, the plasma energy supplied by an external rf source takes the place of the heating to generate the species that subsequently react and deposit on substrate surfaces. Significantly, excessive heating and degradation on the substrate can be avoided by using plasma electron kinetic energy instead of thermal energy. Besides the aspect of generating reactive species at much lower processing

Table 3 Inelastic reactions among reactants, inert gases, and substrate. M refers to the inert gas or substrate, and A, B, and C refer to the reactant gases. From [1].

	A		B
Penning dissociation	$M^* + A_2 \rightarrow 2A\cdot + M$	Collisional detachment	$M^* + A_2^- \rightarrow A_2 + M + e^-$
Penning ionization	$M^* + A_2 \rightarrow A_2^+ + M + e^-$	Associative detachment	$A^- + A \rightarrow A_2 + e$
Ion–ion recombination	$M^- + A_2^+ \rightarrow A_2 + M$ or $M^- + A_2^+ \rightarrow 2A\cdot + M$	Atom recombination	$2A + M \rightarrow A_2 + M$
Electron–ion recombination	$e^- + A_2^+ \rightarrow 2A\cdot$ $e^- + A_2^+ + M \rightarrow A_2 + M$	Atom abstraction	$A + BC \rightarrow AB + C$
Charge transfer	$M^- + A_2 \rightarrow A_2^+ + M$ $M^- + A_2 \rightarrow A_2^- + M$	Atom addition	$A + BC + M \rightarrow ABC + M$

temperatures compared to conventional CVD processing, the ion bombardment can be used to modify film characteristics. Plasma CVD processes can be classified into many subprocesses, such as plasma evaporation deposition, plasma sputtering deposition, plasma ion plating, and plasma nitriding. This classification depends on the conditions of the plasma generated, configuration of the vacuum system, location of the substrate, and type of power supply [19–21]. Plasma-assisted CVD processes for semiconductor processing are generally carried out at pressures of 1 mTorr to 20 Torr substrate temperatures in the range of 100 to 500°C, rf power densities <0.5 W-cm^{-2}, electron densities of 1.0×10^8 to 1.0×10^{12} cm^{-3}, electron mean free paths of <0.1 cm, and average electron energies of 1 to 6 eV.

When the plasma initiates, energy from the rf electric field is coupled into the reactant gases via the kinetic energy of a few free electrons. These electrons gain energy rapidly through the electric field and lose energy slowly through elastic collisions. The high-energy electrons are capable of inelastic collisions that cause the reactant gas molecules to dissociate and ionize, producing secondary electrons by various electron-impact reactions. **Table 1** lists typical electron-impact reactions of silane molecules in an rf plasma discharge. In a steady-state discharge, the electrons generated by electron-impact reactions equal those electrons that are lost to the electrode, walls, and reactive species by attachment and recombination reactions. These reactions have been discussed in detail elsewhere [1, 20, 21].

The two important aspects of a plasma glow discharge are the nonequilibrium low-temperature gas-phase chemical reactions that generate radical and ion reactive species in the plasma discharge, and the flux and energy of these reactive species as they reach and strike the surface of the film being deposited. The bombardment of the ionic species on the surface of the film, which controls the surface mobility of the precursor, is the predominant factor in determining film composition, density, stress, and step coverage or conformality at the relatively low temperatures used in plasma CVD. Reactant gases similar to those used for thermal CVD processes are used for plasma CVD to deposit silicon-based dielectrics at lower deposition temperatures.

Table 4 Heterogeneous reactions between plasma and surface. S refers to the surface in contact with the plasma, and A and B refer to the reactant gases. From [1].

Atom recombination	$S - A + A \rightarrow S + A_2$
Metastable de-excitation	$S + M^* \rightarrow S + M$
Atom abstraction	$S - B + A \rightarrow S + AB$
Sputtering	$S - B + M^+ \rightarrow S^+ + B + M$
Surface contact ionization	$S + B^* \rightarrow B^+ + e^- + S$

• *Reaction kinetics*

Reactions during plasma deposition are complex and not completely understood. Elementary reactions that occur in a plasma have been discussed by various authors [70–73]. The initial reaction between electrons and reactant gas molecules or between reactant gas molecules in a plasma can be classified as elastic or inelastic. In the elastic collisions, only minimal translational energy transfer occurs between the gas molecules and reactant gases. For plasma processing, the elastic collisions play a less important role in reactant dissociation. Significantly more translational, rotational, vibrational, and electronically excitational energy transfer occurs in the inelastic collisions. The major inelastic reactions among electrons, reactant gases, and surface that occur during plasma-assisted CVD processing are typically represented in **Tables 2–4**. Some of the inelastic collisions between inert

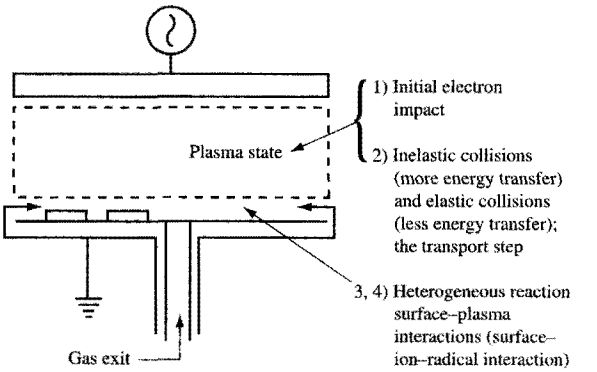


Figure 2

Four steps that characterize the mechanisms of a plasma CVD process. From [1].

gases and reactants (such as helium or argon with silane) significantly affect the chemical nature of the discharge and the properties of the deposited films [74–78]. In many plasma deposition processes, inert carrier and diluent gases such as helium and argon have been used to form a "cooler" plasma, to create more controlled reaction pathways via Penning reactions between carrier and reactant gases [75], and to suppress gas-phase reactions between reactive species. As a result, a plasma diluted with inert gases such as helium can be used to deposit higher-quality insulators. Other fundamental plasma concepts and reactions have been discussed elsewhere [18, 79] and are not discussed here.

• *Deposition mechanisms*

One of the major advantages of plasma deposition processing is its flexibility for depositing films with desirable properties. For conventional thermal CVD processing, physical and chemical properties of the deposited film pertaining to its stress, conformality, density, moisture resistance, and gap-fill properties can be altered by changing the composition and/or type of reactive species. In plasma-assisted CVD, this can be accomplished by varying deposition parameters such as temperature, rf power, pressure, reactant gas mixture ratio, and type of reactant. For example, silicon oxide films deposited with TEOS generally show higher step coverage or conformality than those deposited with silane in a plasma-assisted CVD process. For plasma-assisted CVD of silicon oxide films, properties can be modified not only by changing the type of reactive species, but also by the extent of ion bombardment.

In general, the deposition mechanisms for a plasma CVD process can be qualitatively divided into four major steps, as shown in **Figure 2**. Step 1 includes the primary initial electron-impact reactions between electron and reactant gases to form ions and radical reactive species (Tables 1 and 2). Next, in step 2, transport of these reactive species occurs from the plasma to the substrate surface concurrently with the occurrence of many elastic and inelastic collisions in both the plasma and sheath regions, classified as ion and radical generation steps [80]. Step 3 is the absorption and/or reaction of reactive species (radical absorption and ion incorporation) onto the substrate surface. Finally, in step 4, the reactive species and/or reaction products incorporate into the deposited films or re-emit from surface back to the gas phase. Because of their complexity, the latter two steps are the least known and least studied aspects of plasma CVD. Significant roles are played by ion bombardment [81, 82] and various heterogeneous reactions between ions and radicals with the depositing surface in the sheath region. The two steps critically affect film properties such as conformality [83, 84], density, stress [81], and "impurity" incorporation.

Plasma CVD of amorphous and microcrystalline silicon are the most studied plasma CVD processes, with hundreds of publications on their deposition kinetics and mechanisms. The basic gas-phase chemistry of the silane plasma has been studied by various techniques [83, 85–91]. Different mechanisms have been suggested for the dominant reaction pathway of silicon deposition. One mechanism describes SiH_3 (silyl) radicals playing a dominant role [87, 92–94], while others describe the decomposition of silane to SiH_2 (silylene) and then SiH_2 insertion into gas-phase SiH_4 to form higher silane species [95, 96] as the main silicon deposition mechanism. The debate on which mechanism dominates is ongoing [97–99]. Others have also studied the silane-based deposition mechanisms of widely used insulators such as silicon nitride [100–104], silicon oxide [84, 105–108], and silicon oxynitride [104]. The deposition mechanisms for the CVD of silicon oxide by organosilicon TEOS precursors have been widely studied and modeled by various groups [108].

• *High-density plasma chemical vapor deposition (HDP CVD)*

HDP CVD processing usually includes simultaneous deposition and etching. The ratio of the deposition and sputtering rates (D/S) determines the gap-fill capability of the process. If the ratio is too small, corners of the features to be filled can be sputtered off (this is normally referred to as "corner clipping"). If the ratio is too large, voids or weak seams can form. Surface modeling of the HDP CVD process has been carried out, and a set of mechanisms proposed [109]. The three principal mechanisms are ion-assisted plasma deposition, argon

sputtering, and redeposition of the sputtered material. In HDP CVD, a high-density plasma source [110] [such as inductively coupled plasma (ICP), electron cyclotron resonance (ECR), or helicon] excites a gas mixture that includes silane, oxygen, and argon. The substrate is negatively biased to attract energetic positive ions toward the wafer surface, where oxygen reacts with silane to deposit silicon oxide, and argon removes the silicon oxide by sputtering. The sputtering rate at the corner of a gap is much higher than that on horizontal and vertical surfaces, preventing the gap from being "pinched off." Furthermore, a high degree of near-vertical ion bombardment also limits film deposition on the sidewalls of a gap or other feature. Relatively low reactor pressures (under 10 mTorr) are required to reduce ion scattering and maintain anisotropy, resulting in "bottom-up" deposition filling, as illustrated by Korczynski [111]. Through the use of a high-density plasma source and despite the use of a low reactor pressure, the electron density in HDP CVD may be as high as 5.0×10^{11} cm^{-3} compared to 5.0×10^{9} cm^{-3} in conventional PECVD. Sub-half-micron microelectronic device fabrication has generated many new requirements for high-aspect-ratio fill, enhanced thin-film properties, and improved process control [112]. As a result, a new generation of HDP CVD equipment and processes has been introduced [113]. There are many publications [113–125] regarding HDP plasma sources and the application to CVD gap-fill processing for ULSI fabrication. ECR [114–119], helicon [120, 121], and ICP sources [122, 123] have been used for CVD processes. Readers interested in more details on HDP sources for etching and CVD semiconductor applications should examine two recent books dedicated to this topic [124, 125].

Reactor designs and process optimization

A number of production reactors of diverse types are available for plasma-assisted CVD. Sherman [23] has discussed earlier production reactors, including radial plasma CVD reactors and hot-tube plasma-assisted CVD reactors. These reactors functioned in batch mode. Later, single-wafer processing replaced batch-mode processing because of the capability of clustering both deposition and etch processes in the same system and also because relatively high power densities could be achieved in a single-wafer chamber. This led to the development of dielectric layers of improved quality because the higher power density facilitated the achievement of complete reactions. Parallel-plate PECVD systems operating in either the single-wafer [126] or multistation deposition mode [127, 128] are examples of reactors which are expected to be the mainstay of the future for conventional PECVD processing. Typical PECVD equipment improvement programs include activities to minimize equipment-consumable materials and parts, improve wafer throughput and film uniformity, reduce film particulates, and eliminate plasma damage to layers and devices that may be present on the wafer. Current research and development activities in reactor design include efforts on *in situ* and real-time diagnostics for process control [129, 130], modeling and simulation of reactor design and control [131], and scaling the size of reactors up to 300 mm [132].

One of the main problems in plasma processing is parameter control in a large reactor volume. Since the plasma system is complex, it is generally difficult to identify the effects of a specific process parameter. Plasma rf power and frequency, reactant and diluent flow rates, reactant concentration and temperature, all interact with one another, making it difficult to generalize about processes from one tool type to the next. There are three fundamental factors to consider when optimizing a plasma CVD process. First, maintaining plasma stability is important. To maintain a stable plasma, it should be confined between its electrodes and kept away from the walls of its chamber. Second, its density should be optimized for the desired deposition rate and uniformity. This can be done by adjusting the rf power, pressure, and reactant gas flow rates. Finally, wafer temperature and position in a plasma should be tightly controlled, since these influence plasma–surface interactions. Differences in film thickness, film composition, and plasma damage can occur depending on variations in temperature and wafer position [31, 33].

Dielectric film characteristics and semiconductor applications

As already indicated, the physical and electrical properties of dielectric films can be modified by modifying deposition parameters; for example, film stress can vary from tensile to compressive, depending on deposition processes and conditions [133]. In this section, we discuss some of the pertinent points regarding plasma-assisted CVD of silicon-based and carbon dielectric films that we consider important for ULSI applications.

- *Undoped silicon oxide*

For current silicon IC manufacturing, silicon oxide is the most widely used insulator because of its compatibility with silicon and its excellent physical and electrical properties. The original silicon source material for plasma CVD of silicon oxide was silane [134]. Silane oxidizes easily at temperatures less than 500°C, making it an excellent candidate for low-temperature CVD processing. However, this high reactivity made it undesirable in the early IC manufacturing environment. The use of organosilicon compounds, notably TEOS as a silicon source for PECVD silicon oxide, became common in the

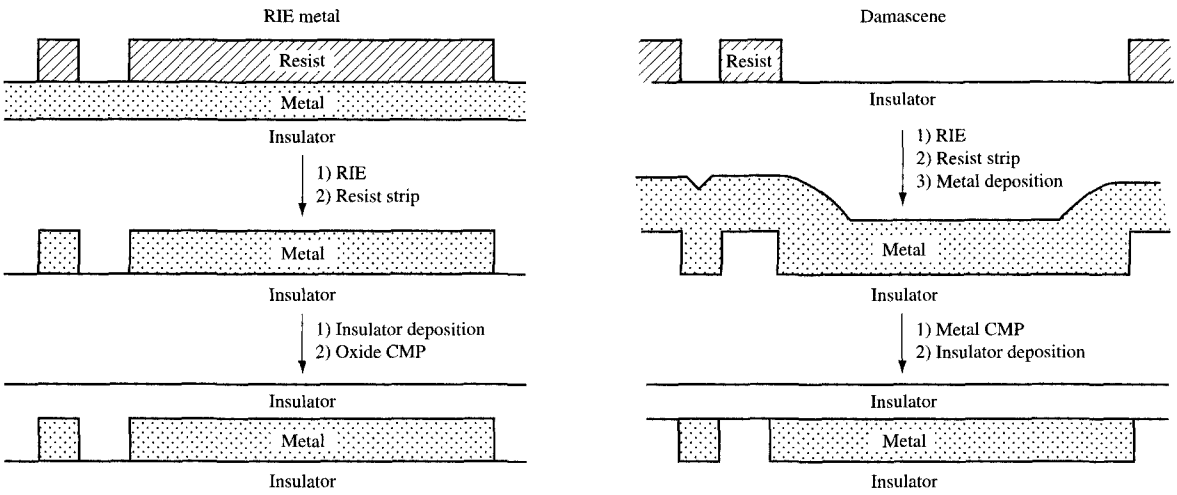


Figure 3

Example process flow for conductor patterning and planarization, comparing RIE-based and damascene-based interconnect schemes. In the RIE-based scheme, the insulator must fill gaps; in the damascene-based scheme, metal lines are formed in the insulator, so that there are no gap-fill requirements for the dielectric with this fabrication method and PECVD oxide is typically used.

1980s [28]. Although TEOS is less reactive than silane and therefore safer to handle, it is a liquid and requires complicated delivery systems. Furthermore, TEOS silicon oxide films display much better step coverage than the silane-based silicon oxide films; this has been fully exploited for gap-fill applications. Silane-based silicon oxide is typically used in applications that do not require gap fill (we refer to these applications as noncritical) such as for hard masks and IMD layers for damascene levels or for less conformal step coverage, as in final passivation.

Damascene IMD applications

Silane-based silicon oxide is typically used in the damascene-based IMD process. The IMD gap-fill problem is eliminated, since the metal lines are patterned, etched, and filled into a planar dielectric, as shown in **Figure 3**. Damascene-based (or simply "damascene") local on-chip interconnections have been used by IBM since the late 1980s and have since gained popularity in the semiconductor manufacturing industry [135]. Damascene interconnections cost less than RIE-based interconnections to fabricate, because both via and metal line levels can be formed with only one metal deposition and one CMP step. This is generally referred to as "dual-damascene" processing [44]. For RIE-based wiring, a separate contact (via) level is typically formed before the metal wiring is formed. The damascene method is extendible to smaller geometries, since the metal shorting issues associated with the RIE-based method are eliminated and the via is self-aligned [44]. Currently, the damascene method appears to be the only commercially feasible method of fabricating submicron copper-based interconnections because of the difficulty of etching copper at that level. Damascene IMD can use conventional PECVD oxide and nitride films, which have much lower cost of ownership than HDP CVD, SOG, or ozone–TEOS gap-fill IMD processes. A critical insulator deposition issue for damascene processing, especially as ground rules shrink, is the inclusion of foreign material (FM) or particles in the dielectric. If a particle were to be left in the dielectric film, it could cause problems at subsequent lithography and oxide RIE steps, as illustrated in **Figure 4**. Prevention of this requires the real-time diagnosis and monitoring of the PECVD equipment.

Gap-fill IMD for BEOL–PECVD dep/etch

In a metal RIE BEOL (back-end-of-line) process, the IMD is considered a critical application, and TEOS-based silicon oxide or silane-based HDP CVD oxide is typically used for enhanced conformality and gap-fill capability, respectively. With each new generation of CMOS technology, the aspect ratio of the metal wiring has increased, making void-free IMD filling at a temperature compatible with the materials properties of the wiring [i.e., under 400°C for Al(Cu)-based wiring] difficult to obtain. A number of techniques have been used by semiconductor manufacturers to solve this problem. In the 1980s IBM pioneered the use of "dep/etch" PECVD IMD [29]. The process consists of alternating PECVD oxide deposition

and argon sputter-etching steps, which taper the as-deposited oxide sidewalls and open the structures for easier dielectric filling. The gap-fill capability of the dep/etch process can be improved by using films with improved conformality. For example, a PECVD TEOS dep/etch/dep process fills higher aspect ratios than a PECVD silane oxide dep/etch/dep process designed with the same film thicknesses and number of etch-back steps, since the conformality of the PECVD TEOS process is about 15–20% better than that of the PECVD silane oxide process.

Al(Cu)-based wiring thickness has been kept approximately constant for the 0.8-μm through 0.25-μm CMOS generations in order to minimize RC (R = metal interconnect resistance and C = interlayer dielectric capacitance) delay. The wiring aspect ratio has increased steadily with each generation, resulting in a higher incidence of voiding between metal lines when use is made of the PECVD dep/etch IMD method. Contacts in sub-0.5-μm CMOS circuits are usually borderless to the underlying wiring. This design technique requires less space for the contact, maximizing wiring density. Thus, if a void exists between the metal wires, the contact can intersect the void. This can result in poor reliability and metal shorting. On the basis of yield and reliability analysis of several CMOS products, we have concluded that the maximum aspect ratio which PECVD dep/etch IMD can fill without creating problems is about 1.2:1.

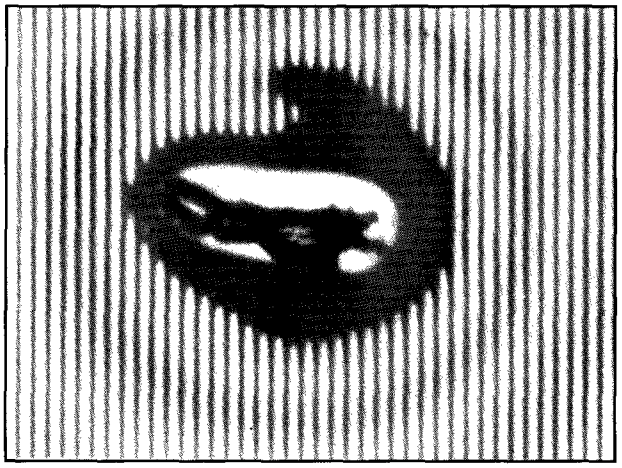


Figure 4

Optical image of a defect caused by a particle that was on a wafer immediately before a damascene-based IMD deposition or was embedded during deposition. Most likely, resist would planarize over the particle, and the resist remaining over the center of the defect would be thinned. This would cause loss of the line pattern, since the particle area would be overexposed, overdeveloped, and too thin to withstand the subsequent RIE processing. Residual metal with no pattern would thus remain in the particle area. The resist would be thicker surrounding the defect, resulting in no etching into the oxide, since the resist would not be fully open to the oxide (underdeveloped and underexposed). Therefore, a circular open area with no metal pattern would remain.

Gap-fill IMD–HDP CVD

In the 1980s, several equipment manufacturers began developing HDP CVD systems for plasma processing, but there were equipment reliability problems (e.g., with their electrostatic chucks and high-speed pumps) that made them difficult to implement in manufacturing [136]. Once these problems were solved in the 1990s, HDP CVD became more attractive because of its superior gap-fill and self-planarization capabilities [115]. A typical IMD sequence involves filling the gaps with the HDP CVD oxide film, followed by a PECVD "cap" layer carried out either in the same or another PECVD system. The dielectric is then polished to the required IMD thickness. The three major issues to consider are wiring reliability, process-induced plasma damage to IC devices, and optimization of the D/S ratio to achieve maximum benefit in both gap fill and planarization.

- *HDP CVD planarization*

As-deposited HDP CVD film profiles are shown in **Figure 5**. Because of the simultaneous deposition and etching inherent in the process, the amount of oxide left on top of metal lines changes with the lateral feature size [137]. As can be seen in the SEM cross-section micrographs, the narrower the line, the less HDP CVD oxide remains on top of the line. This planarizing feature of HDP CVD leads to a reduction of the actual amount of oxide polishing required for the IMD and ultimately to better oxide film uniformity. For example, at the first metal level for a DRAM chip, the majority of the chip area typically consists of narrow lines. Only a small percentage of the wafer contains wide metal lines and features. Therefore, only a small area of the chip would be expected to be covered with the full thickness of oxide after HDP CVD processing because of this lateral feature size dependency. During the subsequent oxide polishing process, the pressure on these wide features should be large (pressure = force/area); therefore, the features with the full thickness of HDP CVD oxide should polish more rapidly. The polishing rate should slow down when the polishing pad hits the narrow lines in the array, since the pressure would then be very low (because of increasing array area). The overall reduction in CMP time required to planarize the IMD leads to improved IMD uniformity and a reduction in the amount of oxide removal required to reach planarity. **Table 5** lists typical via resistance data for wafers processed using dep/etch and HDP CVD. Because of their lower thickness variation after CMP, the

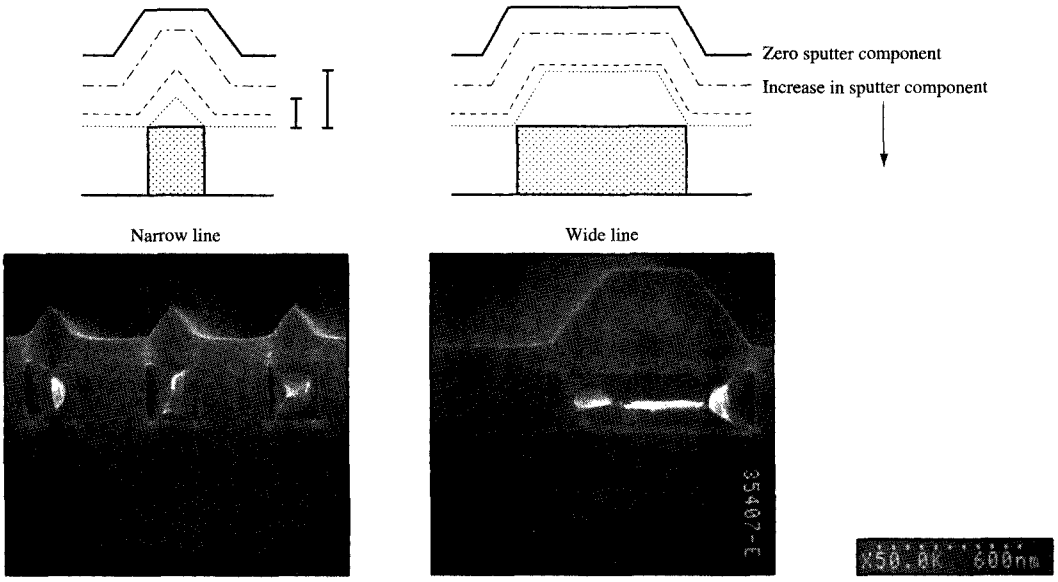


Figure 5

Profiles of an oxide deposited onto metal lines using HDP CVD, illustrating the lateral feature size dependency of the process. The larger the sputtering component or the smaller the *D/S* ratio, the less the oxide remaining on the metal lines and the less the final oxide thickness, especially on the narrow line, as can be seen on the SEM micrographs.

Table 5 Typical normalized IMD via resistance data (98th percentile) for integrated-circuit wafers fabricated using HDP CVD and dep/etch. From [138], with permission.

Via aspect ratio	*Via 1*		*Via 2*	
	HDP	*Dep/etch*	*HDP*	*Dep/etch*
1.33	1.2	1.1	1.1	1.1
	1.0	1.1	1.0	1.1
	1.1	1.1	1.2	1.2
1.67	1.0	1.1	1.1	1.1
	1.0	1.2	1.1	1.0
	1.1	1.1	1.2	1.3
1.91	1.1	1.2	1.1	1.8
	1.0	1.2	1.1	1.2
	1.1	1.3	1.1	1.4

wafers processed using HDP CVD consistently displayed a lower via resistance variation than those processed using dep/etch. In general, via yields decrease as the via aspect ratio increases because of degraded titanium/titanium nitride interconnect liner coverage in the lower portions of the vias [139]. Since the HDP CVD IMD wafers had reduced IMD thickness variation, the variation in via aspect ratio was reduced, resulting in improved via yields.

The smaller the *D/S* ratio or the greater the sputter-etch rate, the more planarization will occur during HDP CVD. In addition, the thicker the HDP CVD film, the better the degree of planarization, as shown in **Figure 6**. Profilometer step height measurements from the array (minimum feature size) to a wide feature were used to characterize the change in planarization with film thickness.

- *Plasma-induced damage*

Recent reports show that HDP CVD silicon oxide for IMD does not cause device degradation in 0.5-μm [119], 0.35-μm [141], and 0.25-μm [123] devices. We have further evaluated HDP CVD plasma-induced damage using integrated CMOS test sites (L_{eff} = 0.2 μm and the thickness of gate oxide = 4–8 nm) and found no differences in charge-to-breakdown and hot-carrier-induced threshold voltage shifts on diode-protected devices. We did, however, observe significant plasma-charging differences when the CMOS gates were not tied to protect diodes, as shown in **Figure 7**. Use of HDP CVD (c) and a high-pressure PECVD dep/etch (b) did not cause significant degradation of the n-FET hot-electron ratio; use of a low-pressure PECVD dep/etch IMD (a) induced significant hot-electron n-FET ratio degradation; use of HDP CVD (c) showed plasma charging on very large

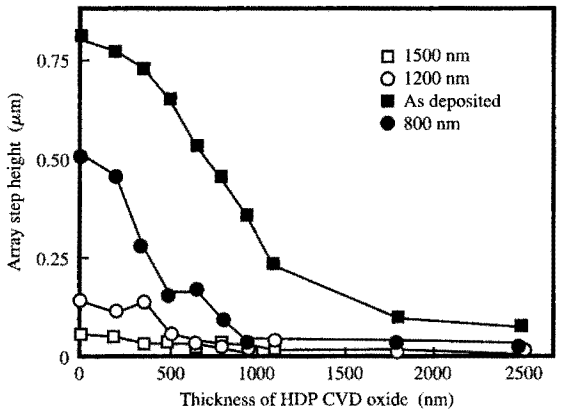


Figure 6

Post-IMD deposition and CMP Al(Cu) line array step height vs. film thickness (HDP CVD oxide thickness + PECVD oxide thickness = 2500 nm) after 0 (as deposited), 800 nm, 1200 nm, and 1500 nm of oxide CMP removal. The HDP CVD was carried out at $E/D = 0.25$; sometimes the ratio of the deposition and sputtering components is expressed by that ratio (etching rate/gross deposition rate), where the etching rate = gross deposition rate − net deposition rate and the gross deposition rate = [thickness$_{unbiased}$ × (1.465/refractive index$_{unbiased}$) × (60 s/min)]/deposition time [140]. From [138], with permission.

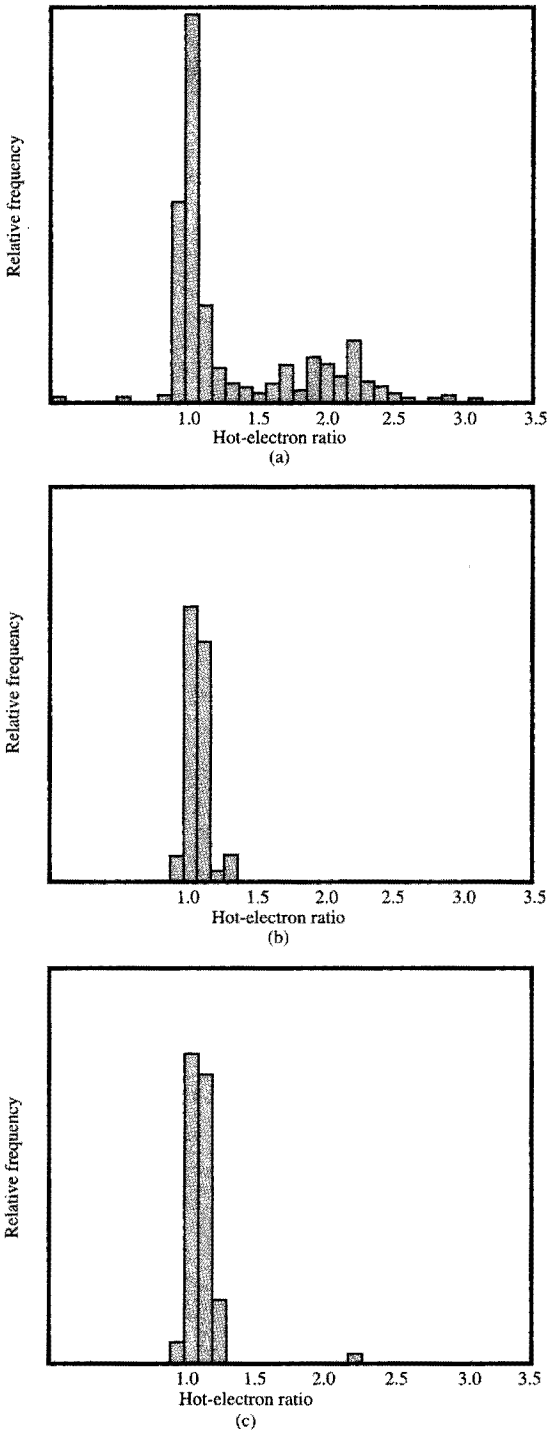


Figure 7

Plasma charging from HDP CVD (using CMOS test sites): n-FET hot-electron ratio for (a) low-pressure dep/etch IMD, (b) high-pressure dep/etch IMD, and (c) HDP CVD IMD. Note that use of the high-pressure PECVD process and HDP CVD eliminates the sporadic charging events. From [142], with permission.

antenna test sites. For a 5-nm gate-oxide thickness and a 10^6:1 antenna ratio, test sites displayed a yield of about 95%. From these data and reported results, plasma-induced damage from an optimized HDP CVD process appears to be comparable to or sometimes better than that of an optimized conventional PECVD process.

• *Aluminum-based wiring reliability*

The temperature variation across the wafer for HDP CVD is larger than in conventional PECVD processing (20–50°C depending on HDP chamber and process). Furthermore, it is known that stress-induced voiding in Al(Cu) thin-film lines can be accelerated by depositing an overlying insulator at higher temperatures [143]. It is therefore important to optimize the HDP CVD process at a temperature that gives acceptable film characteristics, yet does not exceed a temperature that causes poor wiring reliability. Our early 0.35-μm DRAM reliability results showed no resistance shift for HDP CVD processing provided the maximum temperature on the wafer was less than 400°C. Depending on processing conditions, the temperature variation can be as high as 50°C under HDP CVD processing. We observed a center-to-edge variation for metal resistance shifts after stressing which correlated

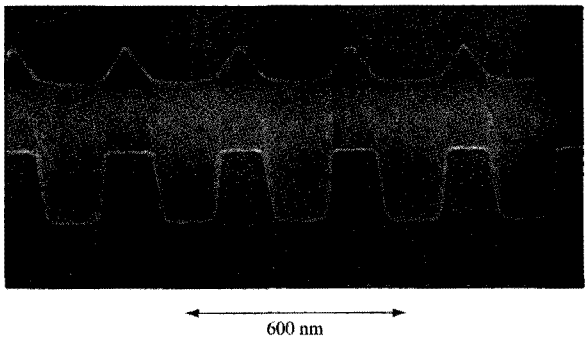


Figure 8

SEM cross section of a 0.175-μm shallow-trench isolation (STI) DRAM array after HDP CVD oxide deposition.

Table 6 Stress-migration-induced resistance shifts for wafers stressed at 200°C and 285°C vs. wafer temperature during HDP CVD. Data were obtained after 1500 hours of stressing at 200°C and 1000 hours at 285°C. The temperature on the wafers ranged from 20 to 50°C depending on processing details; T_{DEP} was the mean wafer temperature during deposition.

T_{DEP} (°C)	*Stress-migration-induced resistance shift* (%)	
	200°C	*285°C*
458	6	17
425	3	3
393	0	0.3

Table 7 CVD equipment trends for gap-fill and damascene IMD films.

CVD process	*1992* (wafers/hr)	*1997* (wafers/hr)
2.0 μm (gap-fill IMD)	10	30
1.5 μm (damascene IMD)	30	80

well with the variation in wafer temperature. When the temperature was greater than 400°C, the resistance of the metal lines was higher. As shown in **Table 6**, a temperature matrix using a 0.35-μm Al(Cu)-based DRAM process indicated that the largest resistance shifts occurred at higher deposition temperatures. Significantly, the HDP CVD process could be optimized to give sufficient reliability results for a 0.35-μm Al(Cu)-based CMOS process and beyond.

Intermetal dielectric development outlook

During the past decade, IMD research and development has focused primarily on the void-free filling of high-aspect-ratio Al(Cu)-based thin-film wires and the planarization of multilevel wiring structures. Void-free filling was difficult to achieve because of the low-temperature restraint [for the Al(Cu)-based wiring]. Planarization was important, since multiple wiring levels were used for submicron technologies [29]. During the past few years, several silicon-oxide-based IMD processes with excellent gap fill have been put into volume manufacturing. With the advent of advanced plasma CVD methods such as HDP CVD and non-plasma methods such as ozone–TEOS CVD as well as SOG, void-free gap fill has become a secondary issue [144]. Planarization has also become less of an issue since CMP has become widely accepted by the semiconductor industry. The principal technology driver for silicon oxide IMD has become "cost of ownership." Manufacturing costs for gap fill and planar IMD films over the past five years have been reduced to about \$10 and \$5 per wafer, respectively [49]. **Table 7** summarizes recent CVD equipment trends for gap fill and damascene IMD films for typical commercial CVD equipment.

Shallow-trench isolation

A critical dielectric thin-film application for the "front end of line" (FEOL) is the shallow-trench isolation (STI) of IC devices [145]. STI is the method of choice for modern integrated circuitry because of its scaling advantages compared to local oxidation of silicon (LOCOS). Traditionally, non-plasma-based dielectric deposition processes such as LPCVD, APCVD, or SACVD TEOS were preferred for this application to eliminate plasma damage to the silicon substrate. However, as ground rules continue to shrink and the aspect ratio continues to increase, new processes for the void-free fill are required. In addition, non-plasma-based TEOS films require high-temperature annealing for densification, which, as IC dimensions shrink, becomes increasingly difficult to implement because of thermal budget limitations.

One of the most recent candidates for the STI gap-fill application is HDP CVD. Various groups have reported results using this technique [123, 146, 147]. The deposition principle is the same as for the BEOL applications mentioned above; i.e., the combination of deposition and simultaneous sputtering leads to a bottom-up filling profile. **Figure 8** shows an SEM cross section of a 0.175-μm DRAM array after HDP CVD STI fill. Note the "huts" formed above the active areas, a typical signature of the *in situ* sputtering. Their height is a function of the *D/S* ratio, the lateral feature size, and the total film thickness, as discussed in the IMD section.

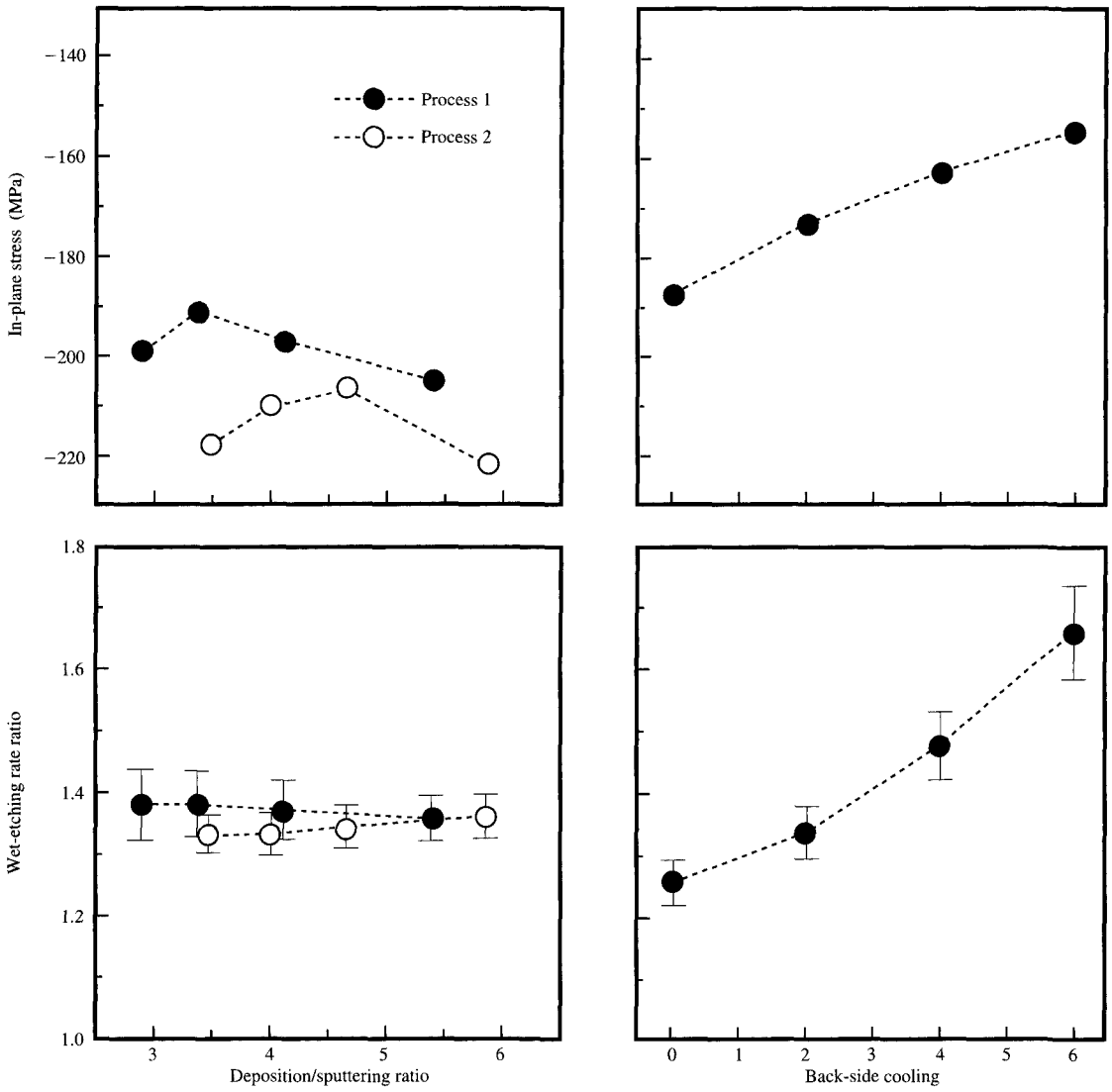


Figure 9

Influence of the *D/S* ratio and the impact of the wafer temperature on in-plane stress and wet-etching rate, normalized with respect to thermally grown oxide.

Another advantage of HDP CVD for STI gap fill is that films deposited by HDP CVD do not require an extra annealing step to sustain subsequent wet stripping and cleaning processes. This arises from both the ion bombardment and the elevated temperature characteristics of the process. In contrast to "back-end-of-line" (BEOL) processing, thermal budget limitations are minimal and deposition at temperatures in excess of 500°C is acceptable. **Figure 9** illustrates the influence of the *D/S* ratio and the impact of the wafer temperature on the in-plane stress and the wet-etching rate, normalized with respect to thermally grown oxide. It is evident that these film properties are determined by substrate temperature. The *D/S* ratio is, however, relevant with regard to void-free gap fill, corner clipping, and substrate damage. The actual challenge for HDP CVD processing for STI is the integration of the film using conventional planarization schemes. Typically, the STI oxide has been deposited

Table 8 HDP CVD film properties as a function of increasing gas flow, wafer temperature, bias rf power, and HDP source rf power; ↑ indicates increasing, ↓ indicates decreasing, and — indicates no change. From [161], with permission.

Parameter ↑	*At.% F*	*Refractive index*	*Stress*	*Uniformity*	*Stability (stress)*
SiF_4 flow	↑	↓	↓	—	—
SiF_4/SiH_4 flow ratio	↑	↓	↓	↓	↑
Temperature	↓	↑	↓	—	↓
Bias rf power	↓	↑	↓	↑	↓
Source rf power	↓	↑	↑	↑	Mixed

using LPCVD, SACVD, and APCVD TEOS oxide processing, which results in conformal films (equal film thickness independent of feature size). The challenge is to optimize and to simplify the planarization scheme, while taking advantage of the unique thickness profile of the HDP CVD oxide.

- *Doped silicon oxide films*

As we have mentioned previously, the properties of dielectric films can be modified by changing reactant chemistry. For example, adding phosphorus and boron to an oxide (BPSG) lowers the melting point of the film such that the material reflows at lower temperatures, enhancing its gap-filling capability. Fluorine can be added to oxide to lower its dielectric constant, making such an oxide a desirable material for the BEOL IMD. There are numerous applications for doped silicon oxide films. We focus our discussion on fluorine-doped silicon oxide (FSG), phosphorus-doped silicon oxide (PSG), and boron/ phosphorus-doped silicon oxide (BPSG) films.

Fluorine-doped silicon oxide (FSG)

FSG films can be deposited by either conventional PECVD processing [148–156] or HDP CVD [157–160]. Such films are of interest because of their lower dielectric constant. Another advantage is that FSG can be deposited with existing PECVD or HDP CVD equipment. Dielectric-constant values of 3.0–3.6 have been reported, but values of 3.5–3.6 are more typical for stable FSG films. The effects of process conditions on silicon tetrafluoride (SiF_4)- and fluorocarbon-based FSG have been extensively discussed elsewhere [154–156]. In general, oxide films doped using SiF_4 as the fluorine source are more stable than those doped using fluorocarbon chemistry [154, 155]. We limit our discussion to FSG films deposited using HDP CVD and compare films deposited using both SiF_4 and carbon tetrafluoride (CF_4) as dopant sources.

In our work, the films were deposited with the use of commercially available 200-mm reactors. We determined that the fluorine content in the films decreased with increasing wafer temperature, increasing wafer bias rf power, and increasing HDP source rf power, as shown in **Table 8**. For example, a variation in wafer temperature of 350–275°C corresponded to a range of 8–16 atomic percent (at.%) fluorine. The films were optimized at a fluorine concentration of 3 at.%; thickness uniformity and fluorine uniformity were 4% and 0.2 at.%, respectively. The dielectric constant measured was 3.5 ± 0.1% for the 3-at.% fluorine films, in agreement with previously published data [154–156].

Multilevel interconnect structures were used to evaluate the FSG film as an IMD. In conventional tungsten plug technology, a titanium layer is used to improve electrical contact to underlying Al(Cu)-based lines. Normally, this titanium (Ti) layer is covered with titanium nitride (TiN) so that the free fluorine from the tungsten reactant gas (tungsten hexafluoride) does not attack the Ti to form

Table 9 Via resistance distributions for integrated-circuit lots showing median (50%) and either 90th or 98th percentile (90/98%) values. The data were normalized to the median via resistance of the SiO_2 control cell. A failure was assumed to have occurred when the 90/98% value was 75% or more higher than the control cell median; at least six wafers per lot were tested. From [161], with permission.

Process	*SiF/SiO ratio (%)*	*Number of lots*	*SiO_2 control*		*SiOF*		
			50%	*90/98%*	*50%*	*90/98%*	*% Fails*
Undoped SiO_2 control	0	43	1	1.2	—	—	5
HDP CVD CF_4	3	7	1	1.2	1.3	2.4	71
HDP CVD SiF_4	3	25	1	1.3	1.0	1.3	4
HDP CVD SiF_4	12	2	1	1.4	1.6	3.0	50
PECVD SiF_4 (low O_2:TEOS)	3	3	1	1.1	1.2	2.2	67
PECVD SiF_4 (high O_2:TEOS)	3	6	1	1.2	1.0	1.2	0

titanium fluoride (TiF_x). (The formation of TiF_x results in poor tungsten adhesion.) If fluorine from the FSG IMD should diffuse into the titanium liner to form TiF_x, the same adhesion problem would occur, resulting in increased via resistance and degraded wiring line reliability. It has been reported that the fluorine in FSG films becomes unstable above a content of 4% Si–F/Si–O [153–155]. Using integrated BEOL wafers, we evaluated SiF_4- and CF_4-doped HDP CVD processes for forming FSG films [161]. **Table 9** summarizes the via resistance distributions obtained for several integrated circuit lots. Wafers processed with CF_4-doped or 12% Si–F/Si–O SiF_4-doped FSG displayed a significantly larger via resistance variation, as shown by the 98th percentile and higher median values, compared to the undoped silicon oxide control wafers. Standard Ti/TiN was deposited in the vias (as a liner) before CVD tungsten filling. We attribute the increased via resistance to poor Ti adhesion. The via resistance distributions of test sites processed with the 3% Si–F/Si–O SiF_4-doped films were not degraded. FSG wafers having low medians and standard deviations for via resistances measured before stressing displayed much lower resistance increases after stressing (and behavior equivalent to that of undoped silicon oxide) than FSG wafers having higher medians and standard deviations [161]. Other reliability data (electromigration, thermal cycling, and temperature/humidity/bias stressing for corrosion) showed that 3% Si–F/Si–O SiF_4-doped films were equivalent to undoped silicon oxide [161]. On the basis of these results, the minimum relative dielectric constant for stable FSG films appears to be 3.5 (at the 3-at.% doping level). By comparison, PECVD silicon oxide has a relative dielectric constant of 4.1. If the line pitch and width are kept constant, the use of FSG decreases the *RC* wiring delay by about 13%. We have fabricated integrated multilevel finger capacitor BEOL test sites to measure the line-to-line and level-to-level capacitance. The measured *RC* delay data shown in **Figure 10** are in excellent agreement with predicted values.

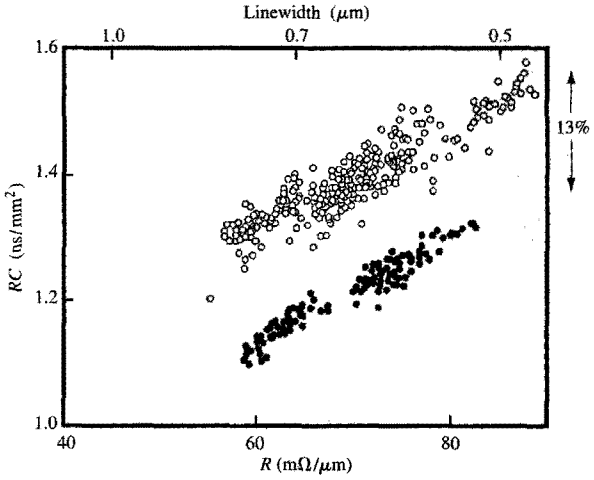


Figure 10

Measured *RC* delay vs. linewidth for 1.44-μm pitch, 45-mΩ/□ sheet-resistivity wiring insulated with undoped silicon oxide (open circles) and FSG that was deposited using HDP CVD (solid circles). From [161], with permission.

Phosphorus-doped and boron/phosphorus-doped silicon oxide (PSG and BPSG)

Phosphorus-doped silicate glass or PSG [3–8 weight % (wt.%) P] is used as the passivation layer over the polysilicon gate conductor (referred to as the premetal dielectric or PMD) in a field-effect transistor (FET) device. The device-related requirements for the PSG process are void-free gap fill (between the gate-conductor lines), high density and stability of the PSG layer (preferably as-deposited); and conformance with a limited thermal budget for the deposition process and any subsequent densification step (e.g., less than 25 minutes at 700°C for advanced logic and less than 25 minutes at 750°C for advanced memory applications). PSG films may have to be reflowed to achieve void-free gap fill, depending on the aspect ratio of the feature. Boron (and/or other dopants such as germanium) [29] must be added to the PSG matrix to reduce the reflow temperature below 1000°C.

PSG and BPSG can be deposited via any number of methods, including non-plasma processes such as APCVD and SACVD, LPCVD, and plasma processes including PECVD and HDP CVD. Although recent advances in doped ozone–TEOS silicon oxide such as SACVD PSG—including the use of higher deposition temperatures (600–650°C) and pressures as high as 700 Torr—have increased the maximum aspect ratio to about 3 for void-free gap fill [see **Figure 11(a)**], further advances in AP or SACVD PSG to provide void-free filling of features having an aspect ratio of 5–6 (0.18-μm DRAM generation) appear difficult within the constraints outlined above. Through the addition of 4–5 wt.% boron and a subsequent 750–800°C atmospheric or higher-pressure steam anneal, void-free filling of higher-aspect-ratio features [see **Figure 11(b)**] becomes feasible, albeit with disadvantages (compared to as-deposited PSG) of increased cycle time, increased thermal cycle, crystal defects [162], and process complexity. Furthermore, the successful use of a reflow temperature below 750°C appears unlikely even with the addition of germanium [29].

PECVD PSG was used in early DRAM (1Mb) chips, but was supplanted by the APCVD BPSG process owing

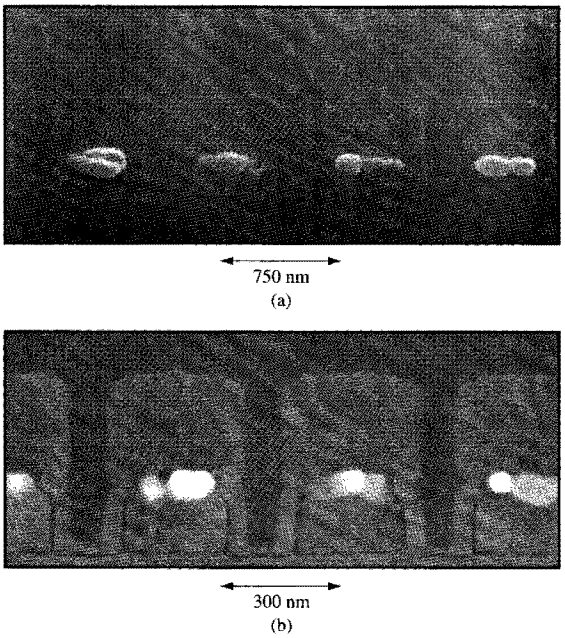


Figure 11

SEM cross-section micrographs showing high-aspect-ratio gap fill for thermal (non-plasma) (a) ozone–TEOS SACVD PSG; (b) ozone–TEOS SACVD BPSG (post-800°C 10-minute steam anneal).

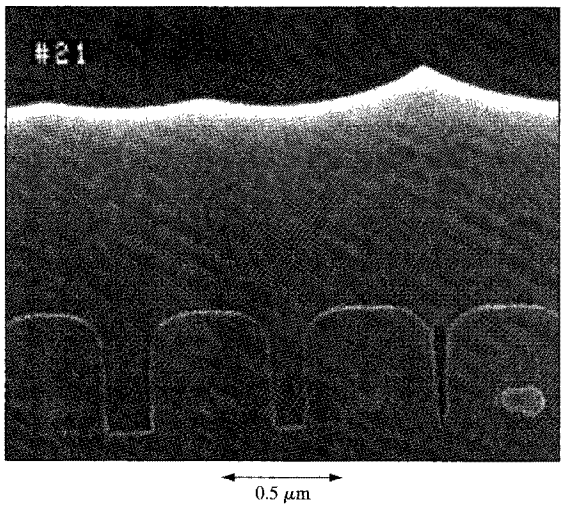


Figure 12

SEM cross-section micrograph showing gap fill of 0.1 μm, 4:1-aspect-ratio features by means of PSG deposited using HDP CVD.

to the better gap fill of the reflowed material. The use of transition-metal silicides as gate-conductor material or in junctions has limited processing temperatures to less than 800°C and forced development of dep/etch PECVD PSG and, subsequently, dep/etch SACVD PSG. Nevertheless, although providing an improvement to gap fill, vertical features with an aspect ratio greater than 1.5 cannot be filled with even a five-step dep/etch sequence [29].

Further advances in high-aspect-ratio gap fill with undoped and phosphorus-doped silicate glass have been achieved in the past two to three years using HDP CVD [136, 163–166]. Void-free gap fill has been extended to features having aspect ratios greater than 3 as a result of the simultaneous deposition and etching inherent in the process. In phosphorus-doped HDP CVD, the gas mixture includes oxygen, argon, silane, and a phosphorus source such as phosphine. Publications on process characterization and integration have thus far been limited [162–165]. Gobil et al. [163] have characterized PSG films deposited in an HDP CVD reactor. In their work, a postdeposition densification at or above 700°C was shown to be required to fully oxidize free phosphorus, degas trapped moisture, and stabilize the film. The D/S ratio was not defined for the parameter space studied, and the structure filled with the PSG was not especially difficult to fill because its sidewalls were tapered at a 45° angle. Qian et al. [164, 165] have discussed the integration of an HDP CVD undoped silicon oxide layer as part of a PMD stack consisting of a PECVD nitride liner with the HDP CVD layer used for gap fill. The effect of possible plasma damage by the HDP CVD process was not discussed.

We have investigated the hardness of HDP CVD films and compared their hardness to that of other gap-fill dielectrics such as SACVD PSG, SACVD BPSG, LPCVD BPSG, and annealed SACVD BPSG. As indicated in **Table 10**, we found that the HDP CVD oxides are harder than the ozone–TEOS and LPCVD oxides, thereby offering a potential advantage in reduced scratching during CMP.

Recent efforts to optimize the deposition of PSG using HDP CVD have resulted in void-free filling of 0.1-μm-wide features having an aspect ratio of 4; this was achieved without corner clipping using typical conditions indicated in **Table 11**. Although the PSG polished at a lower rate (~240 nm/min) than annealed BPSG (~300–400 nm/min), planarization could be accomplished by CMP without difficulty, as indicated by the micrograph shown in **Figure 12**. The tendency of the HDP CVD process to impart plasma damage to underlying sensitive electrical structures was measured in capacitors with large antenna ratios. Table 11 includes yield data on these structures deposited using the aforementioned process. Minimal plasma damage occurred except at the highest antenna ratio (~10M:1), suggesting that there may be a

Table 10 Hardness of CVD oxides and boron- and phosphorus-doped oxides. SA: subatmospheric ozone–TEOS CVD oxide; LP: low-pressure CVD TEOS oxide; HDP: high-density-plasma CVD oxide; BPSG: borophosphosilicate glass; PSG: phosphosilicate glass; USG: undoped silicon oxide.

CVD type	*Sample*	*B and P concentrations* (wt.%)	*Thickness* (μm)	*Deposition temp.* (°C)	*Annealing temp./time* (°C)/(min)	*Hardness* (GPa)
SA	BPSG	4.5, 4.2	0.95	480	N/A	4.4
SA	BPSG	4.6, 4.0	1.02	480	800/25	5.3
SA	PSG	0.0, 4.0	2	600	N/A	4.1
LP	BPSG	4.5, 4.2	0.95	800	800/25	5.9
LP	BPSG	4.5, 4.2	0.95	850	850/25	6.2
HDP	PSG	0.0, 4.5	2.1	<500	N/A	7.1
HDP	USG	N/A	2	<500	N/A	8.3

Table 11 Typical conditions for depositing PSG films using HDP CVD and typical resulting film properties.

Parameter	*Parameter setting*	*Film properties*	
		Property	*Magnitude*
Oxygen (sccm)	100–300	Phosphorus content (wt.%)	5 (range: 0.3)
Argon (sccm)	25–100		
SiH_4 (sccm)	20–75	Deposition rate (nm/min)	600
50% PH_3 in SiH_4 (sccm)	20–75	Polishing rate (nm/min)	240
Low-frequency (400 kHz) power (W)	3500	Within-wafer uniformity (% 1 sigma)	3.2
High-frequency (13.56 MHz) power (W)	2000	Refractive index	1.465
Etch-to-deposition ratio	0.17	Stress (1×10^9 dyne/cm^2)	−1.4
Pressure (mTorr)	<10	Shrinkage after 900°C, 30 min N_2	<0.2%
		Antennae yields (%) at antenna ratio:	
		214K	97.5
		9.7M	87.5

problem for more sensitive, thinner gate-oxide devices. More extensive studies must be done with both test structures and actual device wafers to better understand the extent of such plasma damage.

• *Silicon nitride and silicon oxynitride films*

In this section, some work on PECVD silicon nitride and silicon oxynitride is discussed. Excellent reviews of PECVD (and LPCVD) silicon nitride [104, 167] and oxynitride films [104] providing characterization results and deposition mechanism discussions have been published. LPCVD nitride is typically used for applications where stoichiometric nitride is required; however, it is deposited at relatively high temperatures (720–780°C). For many ULSI applications, a lower deposition temperature (less than 400°C) is required. Nearly stoichiometric silicon nitride can be deposited at such temperatures using ECR or HDP CVD methods. Gate-quality silicon nitride has been prepared using an ECR remote PECVD method and has been implemented successively as a gate dielectric for GaAs metal–insulator–semiconductor (MIS) FETs [168]. Kotecki and Chapple-Sokol [169] have studied the incorporation of hydrogen in films deposited by the ECR remote PECVD method and found that films deposited at temperatures greater than 350°C were stable (no hydrogen desorption) even after annealing at 920°C. Studies of the dielectric properties of ECR CVD SiN_y films [170] and further process studies, especially with respect to plasma stability [171], have been published.

Conventional PECVD nitride and oxynitride films are typically deposited using silane as the silicon source, ammonia and nitrogen as the nitrogen sources, and nitrous oxide as the oxygen source (for oxynitride). Depending on the gas flows and process conditions, the entire range of nitride to oxide can be achieved with a PECVD process [172], making it easy to tune the process

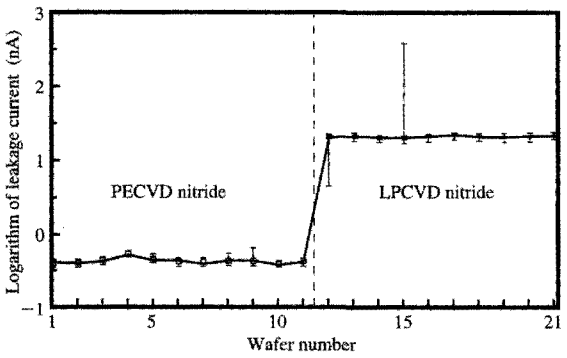


Figure 13

Junction leakage current as measured on different wafers using STI-bounded junction leakage test structures for LPCVD vs. PECVD silicon nitride gate-conductor barrier films. The structures were intended to provide perimeter junction leakage measurements for various devices. The macros consisted of diffusion serpentines having an STI comb perimeter and a 0.2-μm spacing (after diffusion). The comb structure was covered by a gate conductor. The PECVD silicon nitride was 25 nm thick, and the LPCVD nitride was 8 nm thick.

to satisfy photolithography, etching, electrical, and materials requirements. We discuss the following applications for conventional PECVD silicon nitride and/or silicon oxynitride films: final passivation, gate-conductor barrier film, and antireflective coating.

Final passivation

The last dielectric deposited on integrated-circuit wiring is typically designated as "final passivation." A PECVD silicon nitride film serves as both a moisture and diffusion barrier to mobile ions in the final passivation layer [173]. Swann et al. [174] were the first to report the use of PECVD nitride for passivation and have described *C–V* results comparing silicon oxide and silicon nitride sodium contamination as well as silicon device passivation characteristics. Typically, final passivation for semiconductor devices consists of a thin-film stack of PECVD silicon oxide, PECVD silicon nitride, and spun-on polyimide. The dual PECVD silicon oxide and silicon nitride layer has also been used as the passivation layer for solar cells. Nagayoshi et al. [175] have determined that the combination of PECVD oxide and nitride and hydrogen-radical annealing improves the effective lifetime by reducing the surface recombination velocity of the crystalline silicon surface. An important issue for the final passivation in IC fabrication is the total thickness of the PECVD film stack [176]. Typically, it is desirable to maintain a thin oxide and nitride film stack to facilitate etching open "fuses" at the terminal via step. However, if the final passivation becomes too thin, it can crack during chip packaging. Further discussion of such issues can be found elsewhere [177, 178]. Furthermore, the use of PECVD silicon oxynitride has been reported for final passivation [179]. It has also been reported that the diffusivity of sodium in PECVD oxynitride increases with increasing oxygen content [180], but the correct composition provides adequate protection against mobile ion diffusion [104].

Gate-conductor barrier applications

Silicon nitride is typically used as a stop layer for etching contacts at the gate-conductor level because of its high etch selectivity to doped oxides such as BPSG and PSG [37]. The nitride is usually deposited as a thin layer over the gate conductor immediately before the BPSG or PSG is deposited. As mentioned previously, phosphorus in the BPSG and PSG getters mobile ions. Silicon nitride is also an effective mobile ion diffusion barrier. We have previously reported on process optimization of PECVD silicon nitride for the gate-conductor barrier application [181]. Notably, the barrier nitride can affect the surface states of FET devices, and thus their electrical performance [182]. In that work, STI-bounded junction leakage measurements were used to evaluate various nitrides because of the sensitivity of this measurement to surface states. The test structures consisted of diffusion serpentines with an STI comb perimeter and the STI covered by the gate conductor. **Figure 13** shows junction leakage measurements on wafers processed with a PECVD nitride barrier and on wafers processed with an LPCVD nitride barrier. Clearly, the PECVD nitride was more effective at passivating surface states that can cause high junction leakage than the LPCVD nitride. Most likely, the dense structure of the LPCVD nitride lowers the permeability of the film to hydrogen diffusion during subsequent annealing steps [183]. It is important that the barrier film either provide hydrogen or allow hydrogen to diffuse through it in order to passivate surface states and reduce device junction leakage. Although PECVD nitride offers a significant improvement over LPCVD nitride in reducing device junction leakage, the leakage can be substantially changed by varying the stoichiometry of the film. For example, the use of a high-silane flow process to produce PECVD nitride (having a refractive index of 2.0) results in a leakage current comparable to that which occurs for LPCVD nitride, as shown in **Figure 14**. To further improve the barrier film, resulting in consistent low device leakage currents with tight distributions, oxynitride can be used as the barrier in the devices. PECVD silicon oxynitride films act both as a hydrogen donor and as a more permeable layer to hydrogen during subsequent annealing steps [183]. Actually, LPCVD oxynitride (which has a lower hydrogen content than

PECVD oxynitride) can perform the same function given an optimum oxygen content, suggesting that the more open structure of the oxynitride film or higher permeability to hydrogen is the dominant factor in determining the improvement in device junction leakage.

This improvement in leakage behavior may also be due in part to a decrease in the electron trapping rate of the oxynitride or PECVD nitride films. It has been reported that LPCVD nitride displays very strong trapping and hence is considered to be "electron-opaque" [184]. It has also been reported that nitride deposited with excess oxidant displays a weak electron-trapping rate [184]. Most likely, very weak trapping in the PECVD oxynitride makes it a less leaky film. We have found a general relationship between the percentage of Si–H or (Si–H)/(Si–H + N–H) in PECVD nitride and oxynitride films and the junction leakage, as shown in **Figure 15**. The lower the percentage of Si–H, the lower the junction leakage. A nitride film that was deposited in excess oxidant (ammonia) behaved similarly to oxynitride. This illustrates how critical film composition is and how it can markedly influence device characteristics.

The secondary requirement for the oxynitride film is to act as a diffusion barrier to alkali and impurity ions [185]. It is not the primary barrier, since the phosphorus in the BPSG is present to getter the mobile ions. Osenbach and Voris [185] have observed that the diffusivity rate of sodium increases with increasing oxygen content in the PECVD silicon nitride films, suggesting that oxygen-doped films may provide less device protection against mobile ions. Hashimoto et al. [186] have suggested an optimum refractive index range of 1.80 to 1.85 to provide a diffusion barrier to zinc on gallium arsenide substrates. Bonding structural analyses and electrical measurements on PECVD and LPCVD oxynitride films [187, 188] have shown that films with refractive indices of 1.75 to 1.80 have low surface states with minimal leakage. From these reported results and our leakage data, it appears that a PECVD oxynitride film with a refractive index of 1.80 to 1.85 might be desirable for the barrier application. LPCVD oxynitride films can also enhance device performance compared to LPCVD nitride or PECVD nitride films, as indicated in **Figure 16**.

Dielectric ARC applications

Silicon oxynitride dielectric ARCs (antireflective coatings), also designated as ARLs (antireflective layers), deposited using conventional PECVD equipment were first developed to satisfy the antireflective requirements of single-wavelength deep-UV lithography [189, 190]. Traditionally, inorganic ARC solutions include TaSi and TiN [191], TiON [192], hydrogenated silicon (a-Si:H), silicon carbide, and nitride [193]. The widespread emergence of silicon oxynitride ARCs in the semiconductor industry is more recent [25]. Silicon oxynitride films of proper stoichiometry are beginning to

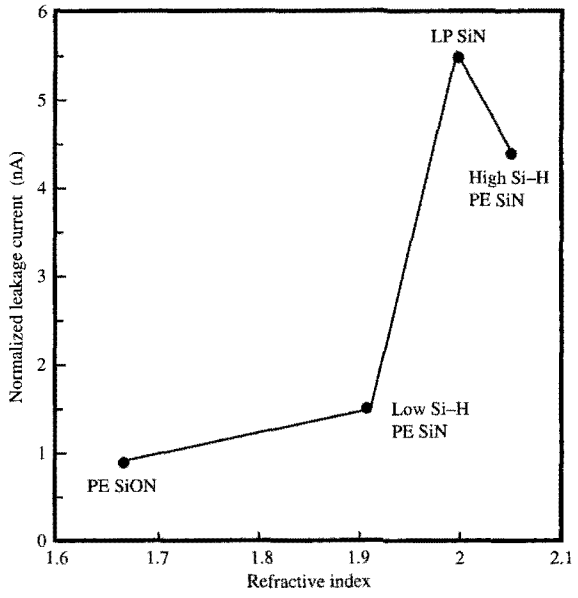


Figure 14

Normalized junction leakage current as measured on STI-bounded junction leakage test structures for LPCVD vs. PECVD silicon (oxy)nitride gate-conductor barrier films of varying stoichiometry and composition.

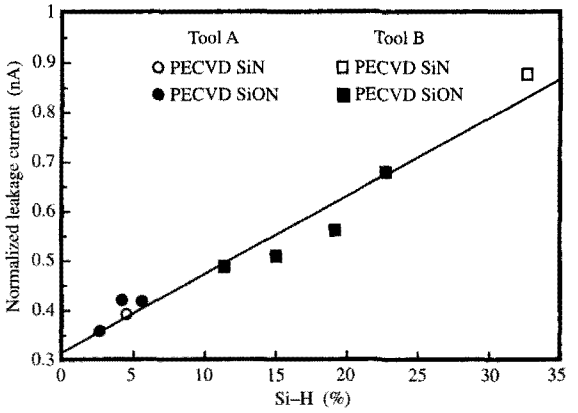


Figure 15

Normalized junction leakage current as measured on STI-bounded junction leakage test structures as a function of % Si–H in PECVD silicon nitride and silicon oxynitride gate-conductor barrier films; % Si–H is defined as (Si–H)/[(Si–H) + (N–H)] × 100. The concentrations of Si–H and N–H were determined using FT-IR.

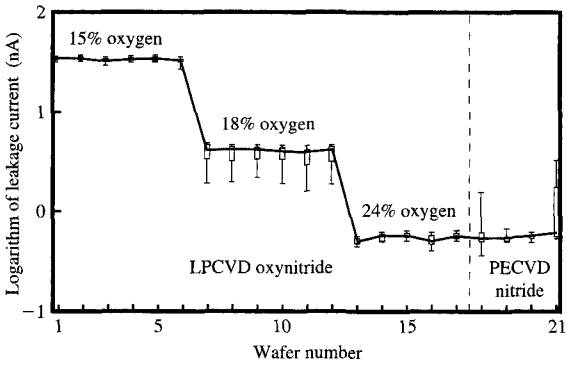


Figure 16

Junction leakage current as measured on different wafers using STI-bounded junction leakage test structures for LPCVD oxynitride gate-conductor barrier films having different oxygen contents, compared to junction leakage current if use is made of PECVD silicon nitride.

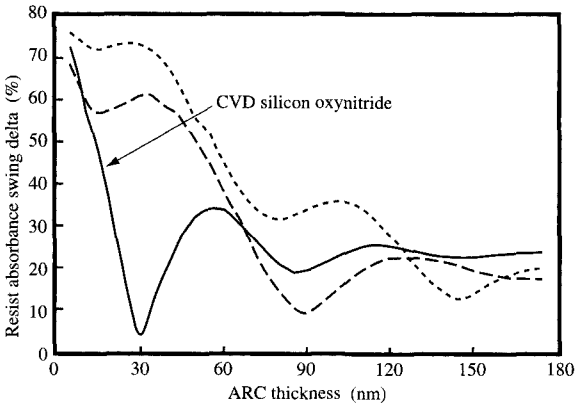


Figure 17

Modeled photoresist absorbance swing variation as a function of ARC thickness for silicon oxynitride CVD (solid curve) and two types of organic ARCs (dashed and dotted curves).

replace conventional spun-on organic ARCs because of their improved conformality, lower cost of ownership, lower defect levels, improved etching selectivity to resist (>3:1), and better optical properties, in addition to the inherent advantage of being suitable for process tailoring with a PECVD process. For dual-damascene processing, there are additional advantages: A single-layer dielectric ARC can be used for both via and line lithography, since it is not stripped with the resist as is organic ARC.

Furthermore, a dielectric ARC can be used as a hard mask (if the etching selectivity is adjusted accordingly), resulting in self-alignment of the vias; this is beneficial at sub-0.25-μm ground rules. As shown in **Figure 17**, a silicon oxynitride ARC can have significant advantages in reducing photoresist swing curves relative to an organic ARC, thus enabling better critical dimension (CD) control.

In general, a CVD silicon oxynitride ARC functions by one of two mechanisms. The first method involves the use of destructive interference, as illustrated in **Figure 18(a)**. Incident light passes through photoresist and is partially reflected at the interface of the resist and ARC. The remaining light passes through the film and is reflected off an underlying substrate back through the ARC film. The CVD silicon oxynitride ARC properties are adjusted such that the reflections at the interface of the resist and the ARC are 180° out of phase and equal in intensity to the reflection from the substrate, resulting in complete cancellation of the light and elimination of undesired resist exposure. Optimal film properties are achieved by varying the film stoichiometry such that the real part of the refractive index (n), the imaginary (k, the extinction coefficient) part of the refractive index, and the thickness are adjusted to meet targets based on optical modeling. Destructive interference is used in applications in which the thickness above the substrate is well controlled, e.g., at the polysilicon gate-conductor (PC) level. A second method of using silicon oxynitride ARC involves the use of light absorption, as illustrated in **Figure 18(b)**. In this case, the thickness between the ARC and the substrate is not well controlled. For example, the ARC film may be deposited directly above an oxide film in which there are significant thickness variations across the wafer, as in damascene processing. Since the path length of the light varies, the ARC film cannot be optimized to result in destructive interference across the entire wafer or chip. However, it is possible to significantly reduce the exposure of the photoresist due to reflections from the interface of the ARC and resist and from the underlying substrate. Reflectance at the interface of the ARC and resist interface is governed by the equation $R = [(n_{ARC} - n_{resist})/(n_{ARC} + n_{resist})]^2$. By tuning the refractive index of the ARC to match that of the resist, these reflections can be minimized. Light that passes through the ARC and is reflected by an underlying substrate can be significantly dampened and virtually eliminated by maximizing the extinction coefficient (absorbance) of the ARC and by depositing an ARC of sufficient thickness.

An example of a CVD silicon oxynitride ARC application is the hard-mask integration method used in patterning polysilicon gate lines. The method involves the deposition of an ozone–TEOS oxide film followed by a PECVD silicon oxynitride film on top of the polysilicon

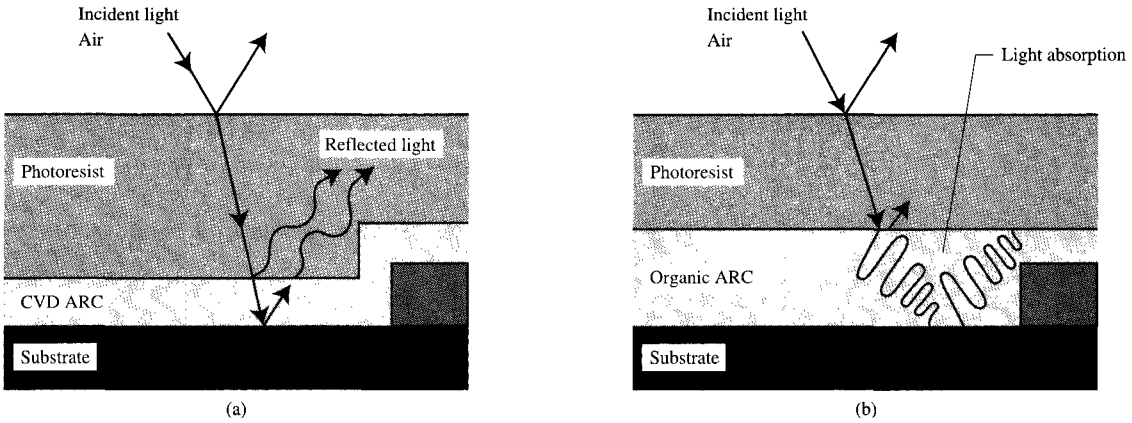


Figure 18

Schematic illustration of functioning of an ARC film, either by (a) destructive interference or (b) absorption.

before photoresist is applied to the wafers. The oxide/ARC stack is capable of conformally covering any underlying topography and the thicknesses are well controlled, so the destructive interference mode can be used. Sensitivity of the resist swing is modeled as a function of thickness in **Figure 19**. In this case, as indicated in the figure, minimal resist swing shift can be obtained at a given target thickness (±2.5 nm).

PECVD silicon oxynitride ARC films require a surface treatment in order to avoid partial exposure of the chemically amplified resists used for deep-UV photolithography. The chemical contamination effects in the processing of chemically amplified resists have been described previously [194]. The migration of basic NH_4^+ ions from the oxynitride film surface into the resist is believed to result in a change of the acidity of the resist. This either leads to "pinching" (undercutting of the vertical resist profile) in negative resists or "footing" (physical extension of the vertical resist profile at its base) in positive resists. The deposition of an oxide cap or oxidation of the oxynitride surface by a plasma treatment can be used to suppress NH_4^+ migration. **Figure 20** shows the effectiveness of an oxide cap, O_2 plasma treatment, and N_2O plasma treatment in eliminating pinching or footing of the photoresist. Resulting PC line profiles are shown in **Figure 21**. As can be seen, the PC lines show superior dimensional control when use is made of the PECVD silicon oxynitride ARC.

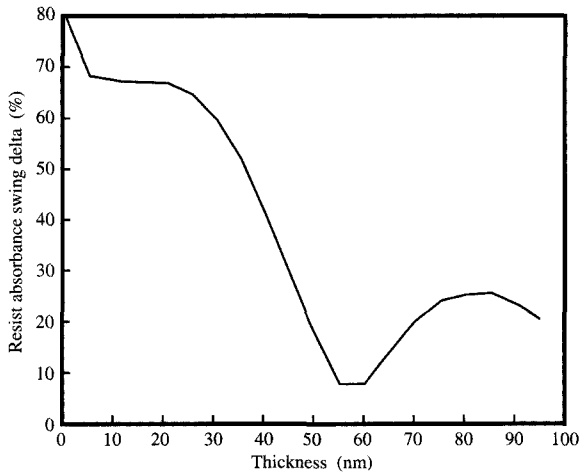


Figure 19

Modeled photoresist swing variation as a function of PECVD silicon oxynitride ARC thickness.

- *Fluorine-doped silicon nitride*

Plasma CVD fluorinated silicon nitride films have been studied as low-hydrogen, low-temperature passivation films for CMOS devices [195] and most recently as a material for dielectric ARC application in the 0.25-μm IC technology [196]. We previously reviewed our work on fluorinated silicon nitride [29]. Stable and highly conformal fluorinated silicon nitride films can be deposited at low temperatures (300–400°C) in a conventional PECVD system using silane, silicon tetrafluoride, and nitrogen as reactant gases. Results from nuclear reaction analysis show that their hydrogen content (4–6 at.%) is less than that of a typical PECVD silicon

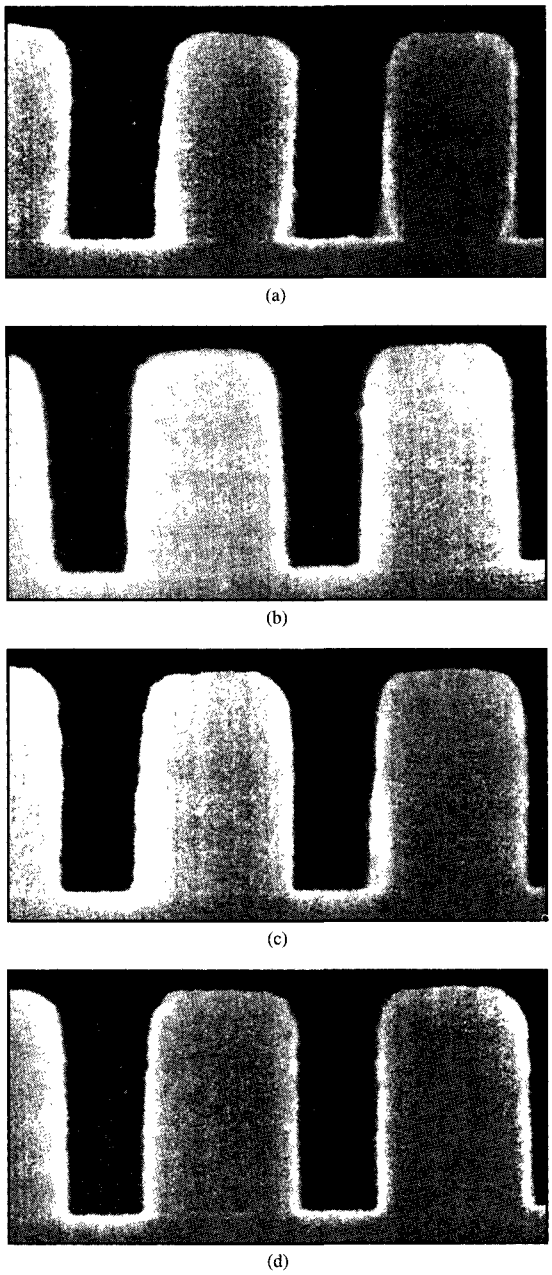


Figure 20

Resist footing for a PECVD silicon oxynitride ARC with (a) no surface treatment; (b) a thin oxide cap; (c) an N_2O plasma surface treatment; (d) O_2 plasma surface treatment.

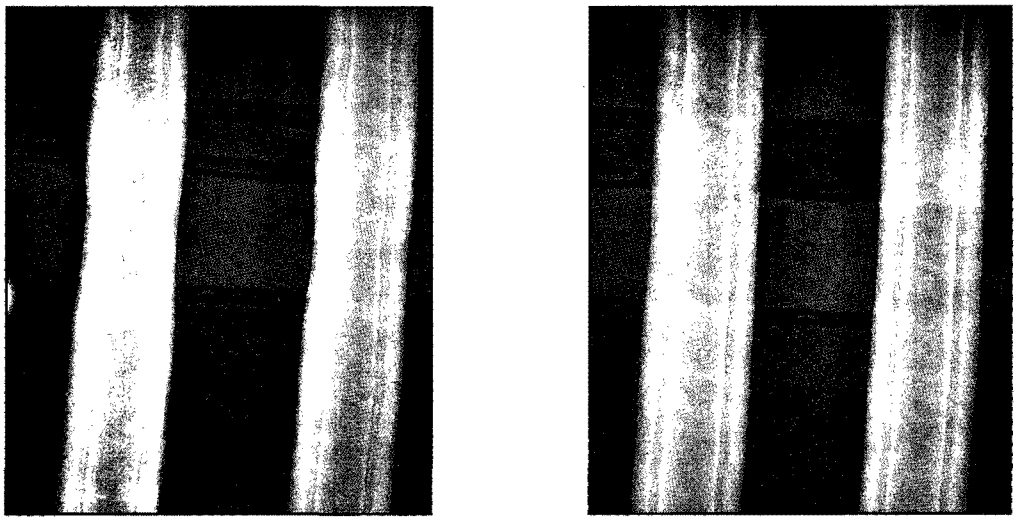
nitride (15–24 at.% hydrogen) film deposited under similar conditions. The Si–H bonds are replaced with Si–F bonds in the PECVD nitride film. Stable fluorinated silicon nitride films have a dielectric constant of 6–6.5, slightly lower than that of conventional PECVD nitride films because of the presence of fluorine. Adding fluorine to a silicon nitride film also enhances its plasma-etching rate [196]. This is important for the dielectric ARC application where the ARC must be removed and a high etching selectivity to underlying films is required. The use of fluorinated silicon nitride films in IC manufacturing has been limited because of adhesion concerns with the incorporation of fluorine in the film, but the improved process margin either with respect to step coverage or etch selectivity may prove to be useful in the future.

- *Silicon boron nitride films*

A review of semiconductor applications for boron and silicon boron nitride films and their deposition (using diborane/ammonia and borazine/nitrogen) can be found in [29]. Boron and silicon boron nitride films have several advantages that make them attractive. First, their high mechanical resistance makes them desirable as polishing stops in CMP [197, 198]. Next, their high RIE selectivity to silicon oxide and silicon nitride [199] makes them desirable in the fabrication of multilevel interconnections. Most recently, silicon boron nitride and silicon boron oxynitride films deposited by PECVD were used to fabricate a single-level test metallization structure with Cu-based wiring [200]. Significantly, it was shown that silicon boron nitride and silicon boron oxynitride are diffusion barriers to Cu, making them potential IMD candidates for Cu-based interconnections. HDP CVD deposition of (cubic) boron nitride with a borazine precursor has been reported [201]. The films thus produced are considered potential candidates for high-power transistor and optoelectronic devices because they can be easily doped and display a high breakdown voltage [202].

PECVD of carbon and fluorine-doped carbon films

For ULSI and gigabit-scale integration (GSI) chips, the performance of the interconnections should preferably match the high performance of the devices [48, 49, 64–66]. As indicated in the first part of this paper, to achieve long-term interconnection performance objectives, low-dielectric-constant IMD will be required. The possible use of fluorine-doped silicon oxide for this purpose has already been discussed. Another possibility is the use of carbon or fluorinated carbon (F–C_x) films [58–63, 203–215]. The dielectric constants of carbon and fluorocarbon films have been reported to be in the range of 2.0 to 3.3, fluorocarbon films being in the lower range. The carbon and fluorocarbon films are generally deposited using individual or a combination of various types of hydrocarbon and fluorocarbon precursors such as methane (CH_4), ethylene (C_2H_4), CF_4, C_2F_6, C_4F_8, CHF_3 with argon and hydrogen [63, 203–205, 207–210]. Ring-type hydrocarbon or fluorocarbon compounds such as benzene



(a) (b)

Figure 21

Top-view SEMs of polysilicon conductor lines formed using (a) conventional organic ARC and (b) PECVD silicon oxynitride ARC. The figure also illustrates the improvement in linewidth control that can be achieved by means of the latter.

(C_6H_6), difluorobenzene ($C_6F_4H_2$), and hexafluorobenzene (C_6F_6) [58, 215] and oxygenated fluorocarbon such as hexafluoropropylene oxide (HFPO, C_3F_6O) [206] have also been used as precursors. Carbon and fluorocarbon films deposited with ring compound precursors are thermally more stable and shrink less upon annealing at higher temperatures than those deposited with linear precursors. The deposition temperatures of these films are typically below 420°C to suppress unwanted diffusion between metal (Al, Cu) and dielectric films. Since low-*k* dielectric properties of carbon and fluorocarbon film are controlled by the film bonding structures and *F/C* (the fluorine-concentration-to-carbon-concentration ratio), the ion bombardment and film bonding structures drastically affect the film's dielectric constant [60, 63, 210].

The properties of carbon films, such as thermal stability, stress, dielectric constant, bonding structures (i.e., sp^3 vs. sp^2 bonding), density and composition (i.e., *H/C* value), are related to deposition conditions (i.e., precursors, rf bias, power density). Carbon films with high sp^2 bond structure and a large *H/C* value tend to have lower dielectric constant and thermal stability [60, 63] than those with a high sp^3 bond structure. The optimization of their adhesion, thermal and chemical stability, stress, and dielectric constant has been investigated [60–63]. The incorporation of a small amount of silicon into carbon films enhances their stability and adhesion to deposited surfaces [60, 208]. However, silicon incorporation increases their dielectric constant. In ULSI device test studies, both carbon- and silicon-doped carbon films have been used as adhesion layers for low-*k* fluorocarbon dielectrics [60, 205, 208]. Carbon films have generally been found to be more thermally and chemically stable than fluorocarbon films.

For fluorocarbon films, the plasma deposition process and precursor chemistry are critical to film stability. In general, films deposited with high *F/C* values tend to have a lower dielectric constant but poorer thermal stability and inferior adhesion. Thus far, the fluorocarbon films examined for ULSI device fabrication have required underlying adhesion layers. Films deposited with feed gases such as (C_2H_2) + C_4F_8 [206], difluorobenzene ($C_6F_4H_2$), and hexafluorobenzene (C_6F_6) + Ar/H_2 [215] display lower dielectric constants and higher stability than films deposited with CHF_3 and/or fluorocarbon gases such as CF_4, C_2F_6, C_4F_8 [203]. The addition of hydrogen or hydrocarbon in the feed gas removes excess fluorine and enhances the crosslinking bonding density in the film [209]. This increases the glass transition temperature of the film and its thermal stability. Recent studies [206, 213] have shown that pulse plasma CVD processing can be used to deposit fluorocarbon films using a hexafluoropropylene oxide (HFPO = C_3F_6O) precursor. By varying plasma pulsewidth, fluorocarbon films having a

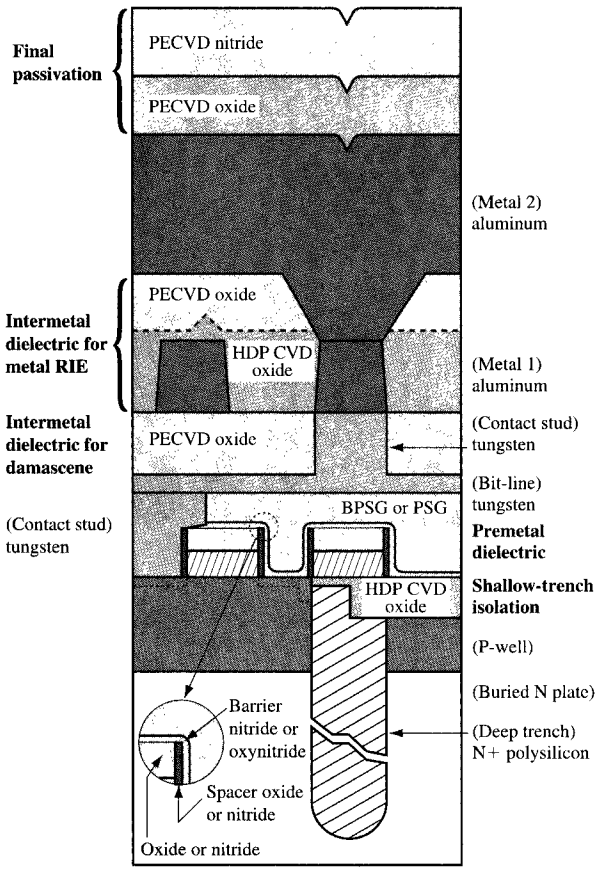


Figure 22

Schematic drawing of a three-level DRAM cell. Potential plasma CVD applications (labeled with bold font) include the shallow-trench isolation, gate-conductor cap, barrier and spacer films, the interlevel dielectric for gate-conductor passivation, the intermetal dielectric for damascene wiring and for metal RIE, and the final passivation. Other potential applications (not shown) might include sacrificial hard masks and antireflective coatings for etching and photolithography applications. From [216], with permission.

low dielectric constant, low dangling bond concentration, and highly stable $-CF_2$ bulk bonding can be deposited. Highly stable fluorocarbon films with dielectric constants as low as 1.95–2.0 can be deposited using this pulse-plasma CVD process.

Thus far, no major advantages regarding carbon and fluorocarbon film properties have been observed for films deposited by HDP CVD versus conventional PECVD. One potential advantage of the former process is its improved gap fill at substrate-bias conditions [205, 208]. In the case of damascene processing, however, this provides no advantage.

Table 12 Summary of potential plasma CVD applications in ULSI-level DRAM and logic chips, and associated deposition process possibilities.

Application	*Process*
Shallow-trench isolation filling	HDP CVD oxide
p-MOS gate conductor passivation	PECVD oxide or nitride
Source/drain implant stop	PECVD oxide or nitride spacers
Premetal dielectric	PECVD nitride or oxynitride barrier + PECVD PSG or PECVD BPSG or HDP CVD PSG
Intermetal dielectric for filling gaps in a metal RIE interconnect	HDP CVD oxide + PECVD oxide cap
Intermetal dielectric for damascene interconnect	PECVD oxide
Final passivation	PECVD oxide and PECVD nitride

Manufacturing issues

A typical CMOS manufacturing process consists of hundreds of separate steps, including a number of low-temperature plasma dielectric depositions. **Table 12** summarizes potential applications and plasma CVD processes relevant to the fabrication of ULSI-level DRAM and logic chips. **Figure 22** is a schematic of a three-level-metal DRAM cell, indicating potential DRAM applications of the processes. A typical ULSI-level logic circuit chip contains five to six metal wiring levels, which may require twice as many plasma deposition steps. The plasma dielectric processes listed in Table 12 are carried out in three types of deposition equipment:

1. Silane-based PECVD for undoped and doped silicon oxide, silicon oxynitride, and silicon nitride.
2. TEOS-based PECVD for undoped and doped silicon oxide.
3. Silane-based HDP CVD for undoped and doped silicon oxide and silicon nitride.

The choice of the type of deposition chamber and/or silicon source depends on the application and the cost. In some cases, non-plasma CVD or spin-on processes can replace the plasma CVD processes.

- *Plasma CVD equipment configuration*

There are several equipment suppliers for plasma CVD processes. One critical manufacturing decision involves deciding which deposition tool platforms to purchase and how to populate the various types of chambers on them. Assuming that a single equipment supplier is chosen for the plasma CVD chambers and tools, the main

manufacturing decision involves the clustering of common plasma CVD processes and multiple process steps. In a declustered manufacturing line, all plasma CVD processes are run separately, with each process running in dedicated chambers. The benefits of declustering are that 1) CVD chamber uniformity and particle levels can be optimized for a single process and 2) process flow is simplified, making it much easier to trace yield-loss problems. In a clustered manufacturing line, common plasma CVD processes, such as silane-based plasma CVD silicon oxide, plasma CVD silicon nitride, and plasma CVD silicon oxynitride, are operated in the same chambers. In addition, where applicable, multiple steps such as the IMD which might include HDP CVD oxide gap fill and a PECVD cap are clustered together on single tool platforms. Clustering has the advantages of reducing the number of tool platforms required and reducing the number of process steps; it has the disadvantage of increasing complexity and reducing the ability to identify yield-loss problems.

Sometimes plasma CVD chambers are dedicated to a particular application because of process temperature and metallic contamination concerns. It is well known that the temperature cycling of CVD chambers produces high particle levels and resulting yield loss. For this reason, it is desirable to keep plasma CVD chambers at a constant temperature. This means that CVD films deposited at different temperatures require chamber dedication. Wafer metallizations [silicide, tungsten, Al(Cu), Cu, etc.] lead to relatively high levels of metallic contamination in plasma CVD chambers. Since premetallization CVD processes, such as STI fill, are extremely sensitive to metallic contamination, additional chamber segregation is required for FEOL and BEOL processes. These temperature and metallic contamination issues increase the number of tool types required and, particularly for small manufacturing lines, increase the total number of tool platforms required and overall cost of ownership.

- *Cost of ownership*

Sematech has pioneered the systematic measurement of wafer cost of ownership; examples for PECVD clean [217] and sputter tool configuration [218] optimization have been discussed. We have summarized the basic Sematech cost model inputs in **Table 13**. Most plasma CVD processes can be performed on tool platforms from multiple equipment vendors, and cost models are used to make purchasing decisions. The cost-model results are highly dependent on the number of chambers placed on the tool platform and how the chambers are regularly qualified for manufacturing. In general, although the tool platform throughput increases as the number of chambers increases, the time during which the tool platform is available for manufacturing decreases because of increased unplanned and planned chamber maintenance. In addition, heavy reliance on monitor wafers to measure film uniformity and particle levels decreases the likelihood of yield loss but increases the overall cost of ownership. **Table 14** shows that the cost of ownership can be significantly reduced by moving from a monitor-wafer-intensive qualification scheme for film uniformity and particles to a product-wafer qualification scheme. The monitor-wafer-intensive scheme assumes that a particle and uniformity wafer is processed after every 50 product wafers are processed in a chamber. The product-wafer scheme assumes processing of a particle and uniformity wafer per day in a chamber, and that a product wafer is measured after 50 wafers are processed in the chamber. Although measuring film uniformity and particles on product wafers increases the complexity of the chamber controls, it also reduces the cost of ownership by about 20% per wafer.

Table 13 Basic Sematech cost model inputs for wafer cost-of-ownership calculation.

1. Hours per day of production
2. Process throughput or cycle time
3. Installed cost of tool
4. Cost of clean-room space, including access areas
5. Payroll costs, including tool operation, maintenance, and engineering
6. Cost of chemical gas and liquids used per wafer
7. Cost of power, water, etc.
8. Cost of spare parts
9. Cost of warranty
10. Cost of monitor wafers required for regular qualifications
11. Cost of monitor and integrated patterned-wafer measurements

Table 14 Comparison of the cost of ownership for a hypothetical system used for plasma CVD of 1-μm-thick silicon oxide films, using monitor wafers vs. actual product to qualify the system.

Parameter (70 wafers/hr)	*Product qualifications*	*Monitor qualifications*
Monitor wafers	0.09	0.60
Measurements	0.01	0.10
Depreciation (personnel, spare parts, chemicals/gases, floor space)	2.23	2.23
Total cost ($)	2.33	2.93

- *Process and equipment extendibility and flexibility*

A common misconception is that semiconductor manufacturing lines are constructed for use by a single generation of IC products. In reality, a manufacturing line

Table 15 1997 Semiconductor Industry Association Roadmap for plasma CVD defect density. From [219], with permission.

		Year						
		1997	*1999*	*2001*	*2003*	*2006*	*2009*	*2010*
Wafer environment	Particle size (nm)	125	90	75	65	50	35	25
	Defect density (m^{-3})	27	12	8	5	2	1	1
On wafer	Particle size (nm)	200	200	200	200	200	200	200
	Defect density (m^{-3})	25	20	15	10	5	1	1

will typically produce two or three full generations with scheduled linewidth shrinkage. For example, a 0.35-μm-generation 64MB DRAM line would cycle through 0.30-μm and 0.25-μm 64MB DRAM and 0.25-μm, 0.21-μm, and 0.18-μm 256MB DRAM with essentially no changes to nonphotolithography tools. This means that plasma CVD tools being purchased must be able to eventually meet much more stringent defect density requirements than initially required. The 1997 Semiconductor Industry Association's Roadmap for plasma CVD film defect density is shown in **Table 15** [219]. A major consideration in selecting tool platform suppliers is their ability to continuously improve the defect density levels in their tools. Some semiconductor manufacturing lines simultaneously manufacture a mixture of memory and logic products. Since the number of films and their thicknesses vary considerably for different types of ICs, having a versatile tool platform and process chambers can also be an important consideration in equipment selection.

- *300-mm-diameter wafer manufacturing*

The most significant challenge for today's equipment and IC manufacturers is the transition from 200-mm- to 300-mm-diameter wafer processing [220]. The International 300-mm Initiative (I300I) and Japan 300-mm Semiconductor Technology Conference (J300) have formulated a set of factory guidelines for process, metrology, and test equipment [221]. In general, the issues regarding 300-mm-diameter-wafer plasma deposition processing are the same for all IC processes. The scaling up of process, metrology, and test equipment to 300 mm is of course challenging by itself and has been successfully demonstrated by a number of equipment vendors. But it is recognized that real-time measurements, *in situ* sensors, and real-time closed-loop control, as well as a capability to obtain process, metrology, and test information, are critical [129, 130]. IC manufacturers must be able to correlate final test yield and performance to specific chips, processes, and equipment [222]. Ideally, process, metrology, and test equipment should maintain the integrity of the wafer order or wafer identification and catalog the process, measurement, and test data for each wafer at each step of wafer processing. In addition, it is expected that 300-mm-diameter-wafer factories will use some type of mini-environment to control contamination levels in their clean rooms [223]. This sophisticated level of factory design and operation is unprecedented, making cooperation between industry IC and equipment manufacturers and conformance to standards set forth by I300I/J300 imperative.

Concluding remarks

We have reviewed the plasma-assisted CVD of dielectric films, with an emphasis on aspects relevant to ULSI semiconductor circuits. In addition, we have indicated that manufacturing needs must be considered early in the process and tool development phase. Obviously, the ultimate goal is to optimize a plasma CVD process for a particular application at the lowest cost of ownership. Future research and development must focus not only on specific technical issues that arise with each new IC generation (such as integration of a stable low-k IMD into the BEOL), but also on manufacturability and cost. With 300-mm-diameter wafers containing sub-0.25-μm semiconductor IC circuits on the horizon, the technical and manufacturing issues are daunting; new challenges are presented to both the semiconductor manufacturers and their equipment suppliers, even for the conventional processes used in IC production.

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