Mater. Res. Soc. Symp. Proc. Vol. 1396 © 2012 Materials Research Society
DOI: 10.1557/opl.2012.880

Performance Comparison and Design Issue on Different GaN Power Transistor Structures

Chwan-Ying Lee[1], Chien-Chung Hung[1], Wei-Hung Kuo[1], Young-Shying Chen[1], Lurng-Shehng Lee[1], Cheng-Tyng Yen[1], Suh-Fang Lin[1], Rong Xuan[1], Tzu-Kun Ku[1], and Ming-Jinn Tsai[1]
[1]Electronics and Opto-Electronics Research Laboratory (EOL), Industrial Technology Research Institute (ITRI), Chung Hsing Rd., Chutung, Hsinchu, Taiwan, R.O.C.

ABSTRACT

Three types of Ganium Nitride (GaN) transistors were studied in this work. The devices were fabricated and exhibited unique characteristics over on-state current and off-state blocking performances. We also compared the performance differences of devices fabricated by multi-epitaxial GaN/AlGaN layers on different substrates (Sapphire and Si) and evaluated the correlations among starting substrate, device variation, and manufacturing uniformity. The first device is a normally-on device with Sapphire substrate which shows good drain saturation current (Idsat) and breakdown characteristics, but the gate leakage current is quite large. The second device is a normally-off GaN transistor named metal-insulate-semiconductor (MIS) heterojunction field-effect transistor (MIS-HFET) which exhibits good performance with threshold voltage (Vth) of 3V and breakdown voltage (Vbd) of over 1800V. However the third device is a normally-off GaN metal-oxide-semiconductor field-elect transistor (MOSFET) structure which is rather difficult to exhibit good blocking characteristic due to inadequate doping process control of the reduce-surface-field (RESURF) region.

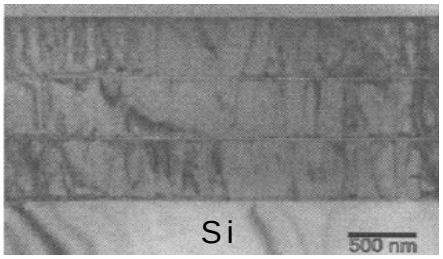
INTRODUCTION

Wide band-gap semiconductor materials, such as Ganium Nitride (GaN) and Silicon Carbide (SiC), have superior properties and have been attracting considerable attention to be used as new generation power electronic devices. GaN device has very high band gap (3.4eV), high critical electric field (up to 3MV/cm) and high saturation velocity (2.5E7 cm/s). Typically, GaN device has simpler process as compared to SiC device, making GaN even more promising for high power, high frequency, and low-cost applications. Many studies [1-4] have been done on AlGaN/GaN based device taking advantage of the two-dimensional electron gas (2DEG) generated at the interface of AlGaN and GaN hetrojunction. However, the Vth is rather difficult to be positive and therefore it usually becomes a normally-on device. The normally-on device can be used for some consumer applications with less safety consideration. However in some applications, such as motor control, the safety operation is the most concern. So, there is a strong requirement that a normally-off device is needed for this type of application. Some improved GaN devices, typically called MIS high-electron-mobility-transistor (MIS-HEMT) or MIS-HFET, adopt gate insulator structure to suppress gate leakage current [5-6] and used RIE method to etch down channel region [7-8] by engineering the 2DEG property to get the normally-off characteristic. This device can have higher breakdown voltage while sacrificing some output performance. The third fabricated GaN device is a typical lateral-channel MOSFET structure [9-10]. It does not have 2DEG advantage, so the on resistance (Ron) will be expectedly higher than that of GaN HEMT or MIS-HEMT device. The purpose of this work is to study and compare the performance and characteristics of various GaN devices so as to find a normally-off

device with better Vbd and Ron performances. We fabricated three GaN devices to investigate and compare their electrical performance and discuss ways to optimize device characteristics to meet the high-voltage/high-power requirements. We also proposed a novel aluminum nitride (AlN) selective-area growth (SAG) technique in order to have carrier modulation and band diagram engineering effect. The target is to achieve a HEMT device with lower Ron characteristic and normally-off performance.

EXPERIMENTAL RESULTS

Two types of GaN substrates were used in this study. One is the GaN on sapphire substrate and the other is a crack-free GaN on Si substrate. Both are used for either normally-on HEMT device or normally-off MIS-HEMT device as for comparison. Figure 1(a) shows a cross-sectional TEM image of a buffer structure of GaN-on-Si substrate by implementing AlN nucleation layer followed by multi-epitaxial AlGaN/GaN buffer layers. The interface of the buffer layers is smooth enough to further grow epitaxial GaN channel layer. In this study, AlN-seed layer is used with low temperature interlayer technology to overcome the problem of insufficient GaN epitaxy thickness due to significant coefficient of thermal expansion (CTE) difference (~ 56%) between GaN and Si. As a result, the GaN epitaxy thickness can be increased up to 3 um grown on a blanket Si substrate and can be increased up to 4 um grown on a patterned Si substrate, as shown in figure 1(b). The patterned structure can effectively release the film stress at local position so as to grow better quality of epitaxial layers.

(a) 

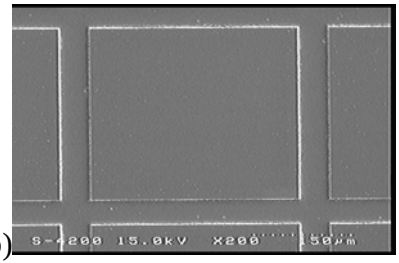
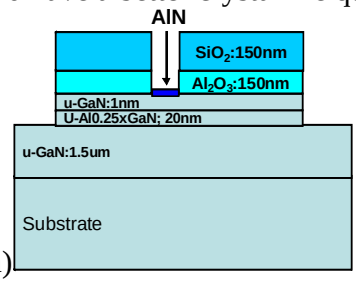
(b) 

Figure 1. (a) Buffer layers of GaN-on-Si structure. (b) Top view of patterned structure.

Figure 2(a) shows a device with AlN SAG process and figure 2(b) shows the SEM image after this regrowth step. The AlN capping layer is selectively grown at the gate region with thickness ranging from 18nm ~ 42nm. As a result, the Idsat increased ~ 40% by the AlN SAG structure due to the carrier modulation effect. However, the Vth didn't become higher. It is possible due to the poor control of epitaxial gas flow in this experiment. In order to have a higher Vth, it's necessary to optimize the epitaxial regrowth process and to make AlN thicker and have a better crystalline quality.

(a) 

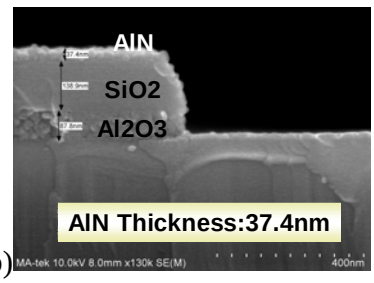
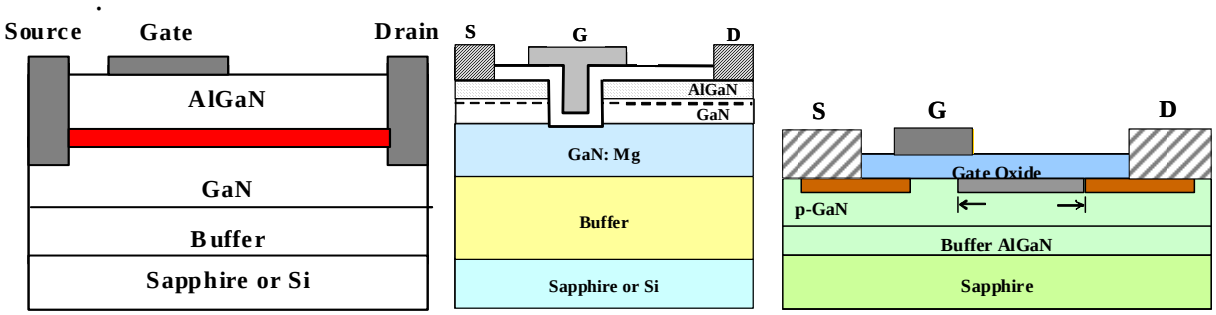
(b) 

Figure 2. (a) GaN device with AlN regrowth process. (b) SEM image after AlN regrowth step.

Figure 3 shows the schematic cross-sectional structures of GaN transistors studied in this work. The GaN HEMT (shown in figure 3(a)) and MIS-HEMT (shown in figure 3(b)) devices are fabricated on both Si and Sapphire substrates, but the GaN MOSFET device is formed on the Sapphire substrate (as shown in figure 3(c)). The thickness of the un-doped GaN channel layer for the HEMT device is designed to be about 2.5 um, and the thickness of the electron supply layer AlGaN is about 20 nm with Al mole fraction of ~ 25% which can piezoelectrically induced charge in the GaN/AlGaN interface and can have a lower turn-on resistance. However, MIS-HEMT and MOSFET devices are preferred in order to have the normally-off characteristic. The carrier density in the 2DEG layer can be adjusted by introducing the recessed gate structure. The recessed structure can engineer the GaN/AlGaN interface configuration and therefore relax the electric field induced by the piezoelectric and spontaneous depolarization effect. Once the carrier density is decreased around the recessed gate region, the channel conductivity can be modulated and hence the Vth can be enhanced to become a normally-off device. However, the control of the recessed gate of MIS-HEMT device is not easy and the Vth of this device is still not large enough and reliable. For better control of Vth performace, the MOS device is also fabricated for comparison. The thickness of the p-type GaN well region is designed to be 1 ~ 3 um and the RESURF region is 0 ~ 20 um long for achieving different blocking performances. Due to the low quality of gate insulator interface and non existence of the 2DEG layer in the MOSFET device, the Ron of this MOSFET device will not expectedly to be very low.



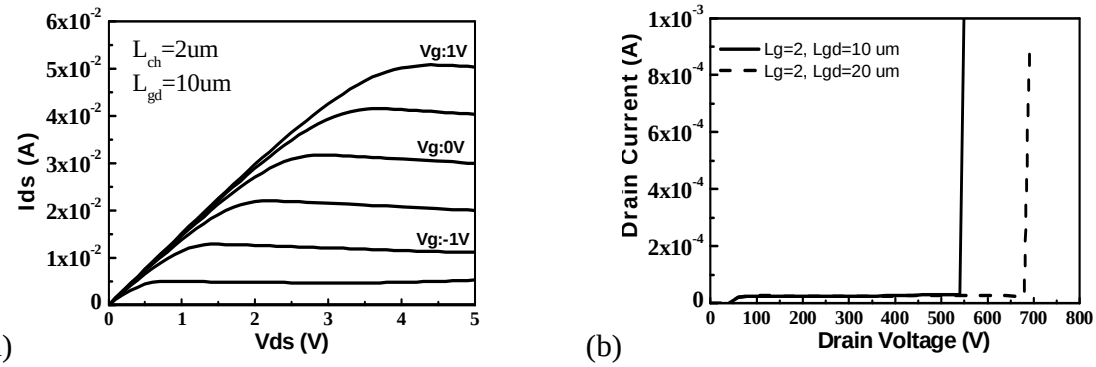
(a) (b) (c)

Figure 3. The cross sectional view of (a) HEMT, (b) MIS-HEMT, and (c) MOSFET devices.

Figure 4 shows the output and reverse blocking characteristics of normally-on HEMT device fabricated on Sapphire substrate. Owing to the high carrier density of 2DEG layer formed between source and drain region, the device can only presents a negative threshold voltage of ~ -3V and the Idsat achieves 30 mA at gate voltage (Vg)=0V for device W/L = 10/2 um. When Vg is applied at 1V, the saturation drain current is about 50 mA, which is corresponding to current density of 150 mA/mm on a device width of 330 um. The Vbd can be achieved up to 700V and the specific-on resistance in the linear region is about 13 mOhm-cm^2. Besides, GaN-on-Si HEMT device is also fabricated and characterized. The Ron and Vbd are similar to that of GaN-on-sapphire device. However, the breakdown voltage uniformity is rather worse for the GaN-on-Si HEMT device. We attribute this bad uniformity to the higher defect density of GaN-on-Si substrate as compared to the lower defect density of GaN-on-Sapphire substrate.

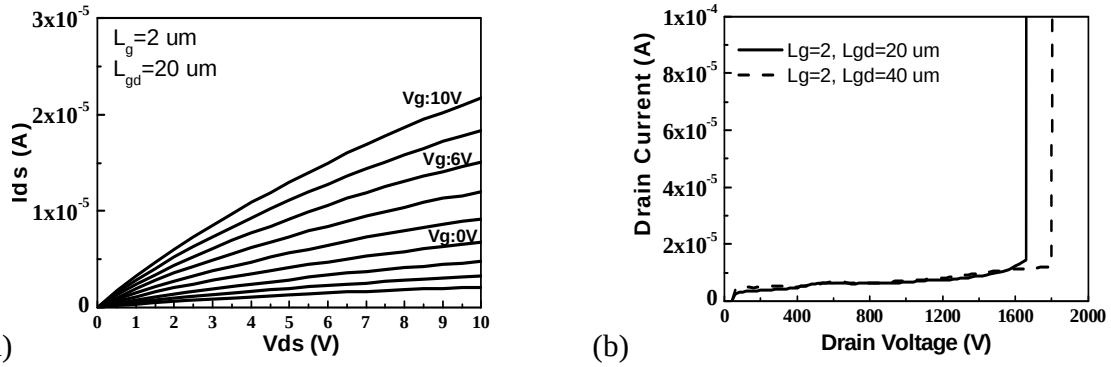
Figure 5 shows the output and reverse blocking characteristics of normally-off MIS-HEMT device fabricated on Sapphire substrate. The device exhibits a fair on-state characteristic of Ids ~ 20 uA at Vds and Vg=10V, as shown in figure 5(a). Although the breakdown voltage

can be higher than 1800V as shown in figure 5(b), the on-state current is much lower than the HEMT device due to the difficulty of recess process controlling and possible damage on the 2DEG structure and therefore it degrades the high mobility property of HEMT device.



(a) (b)

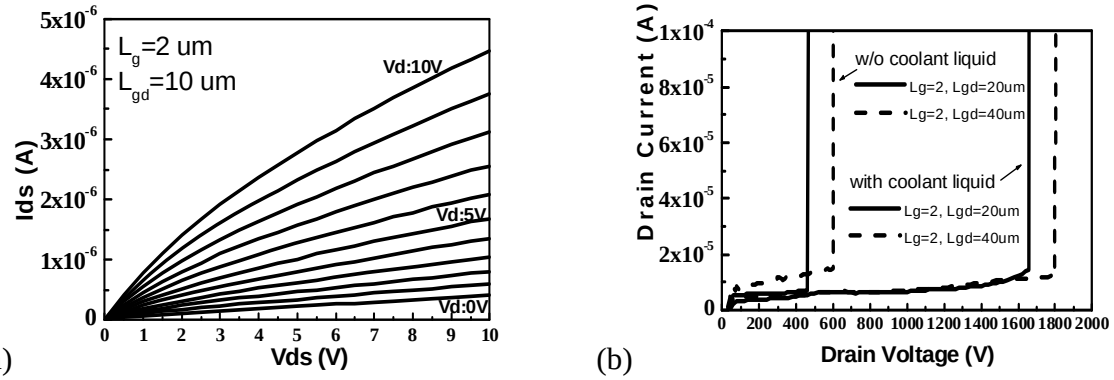
Figure 4. The electrical characteristics of GaN HEMT device. (a) Ids vs. Vds, and (b) reverse leakage current vs. applied voltage.



(a) (b)

Figure 5. The electrical characteristics of GaN-on-Sapphire MIS-HEMT device. (a) Ids vs. Vds, and (b) reverse leakage current vs. applied voltage.

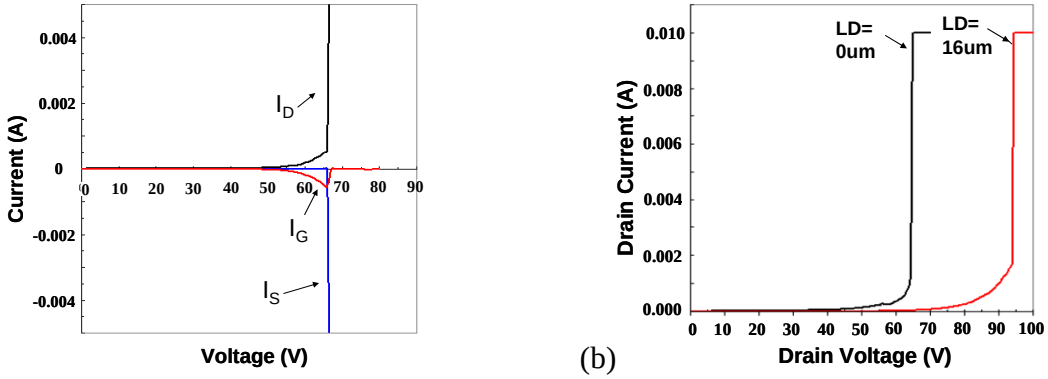
We also compare the MIS-HEMT device performance difference between GaN-on-sapphire and GaN-on-Si substrates. The output and reverse blocking characteristics of the MIS-HEMT device fabricated on silicon substrate can be seen in figure 6. The Idsat current of GaN-on-Si device is one order smaller than that of GaN-on-Sapphire device, as shown in figure 6(a). The possible reasons are variation of recessed gate process, quality of gate insulator, and epitaxial quality of GaN-on-Silicon substrate. The recessed gate may have etched through the 2DEG layer, resulting in the break of channel layer and degradation of channel conductivity. The root cause is still unclear and need to be further investigated. In figure 6(b), we try to measure the breakdown characteristic on MIS-HEMT devices with different testing conditions. We applied the electronics coolant liquids (Fluorinert^{TM} commercialized by 3M) on some devices. It can be emulated to a similar situation that a final product is in a package. This prevents the device from encountering atmosphere arcing under testing. The breakdown voltage is over 1800V with the coolant liquids protected as compared to that of ~ 600V without the coolant liquids protected. The epitaxial module and fabrication process of GaN-on-Silicon device should be further developed and optimized to realize a normally-off and low-cost transistor.



(a) (b)

Figure 6. The electrical characteristics of GaN-on-Si MIS-HEMT device. (a) Ids vs. Vds, and (b) reverse leakage current vs. applied voltage.

As compared to GaN HEMT device, MOSFET device can have a much lower gate leakage current, as shown in figure 7(a), and can have a better gate controllability. The threshold voltage of the fabricated GaN MOSFET device is higher than 6V. However, the on-state capability of MOSFET device is worse than that of HEMT device due to the lack of 2DEG layers. The channel mobility is ~ 19 cm2/V-s for a device channel W/L of 484/4 um at Vg=5V, which implies a poor gate insulator with interface state > 1E12 $eV^{-1}cm^{-2}$ may be formed on the device. Figure 7(b) shows the breakdown performance compared two devices with different drift zone length. The breakdown voltage is only < 100V, far lower than the fabricated HEMT and MIS-HEMT devices. The major issue on this device is because of a high P-GaN concentration of 1E17 cm^{-3} was selected and an unintended N+/P junction breakdown was happened, and therefore a lower breakdown voltage was achieved. We verify the breakdown mechanism on a device simulation by solving drift-diffusion Poisson equation in Synopsys Sentaurus software. It gives a suggestion to use a lower concentrate of 2E16 cm^{-3} in order to redistribute the electrostatic potential contour. A higher breakdown voltage of >500V can be expected in a simulation case as shown in figure 8.



(a) (b)

Figure 7. (a) Gate leakage as compared to S/D current of MOSFET device, (b) Breakdown voltage for devices with different drift zone length.

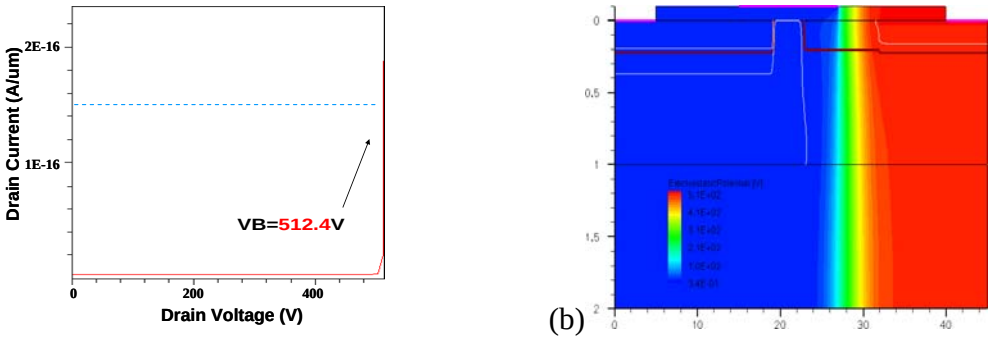


Figure 8. (a) Simulation of reverse blocking capability on a GaN MOSFET device. (b) Electrostatic potential contour at device breakdown point.

CONCLUSIONS

Three types of GaN transistors were fabricated and studied in this work and exhibited different properties over on-state current and off-state breakdown voltage performances. The HEMT device shows Ron of ~ 13 mOhm-cm^2 and Vbd ~ 700V. However, the gate leakage current is quite large and Vth shows negative value of ~ -3V. It is suggested to adapt and further improve the AlN SAG process so as to have a higher Vth performance and better Ron characteristic. Besides, the MIS-HEMT device exhibits good performance with positive Vth of 3V and the Vbd of over 1800V. However, the Ron shows poor performance due to the difficulty of controlling recess process. It is also suggested to improve the gate insulation and epitaxial quality so as to have better characteristic on the on-state property. As to the MOSFET device, it has a lower gate leakage current with better gate control ability. However, the device exhibits low channel mobility of ~ 19 cm2/V-s and low Vbd of < 100V. It is suggested to improve the MOS gate insulator with less interfacial oxide charges and also carefully designed the voltage-blocking RESURF doping conditions.

REFERENCES

1. H. Kambayashi, Y. Satoh, T. Kokawa, N. Ikeda, T. Nomura, and S. Kate, *Solid State Electronics*, **56**, 163-167 (2011).
2. T. Oka and T. Nozawa, *IEEE Electron Device Letters*, **29**(7), 668-670 (2008).
3. D. Kikuta, J.-P. AO, J. Matsuda, and Y. Ohno, *IEICE Trans. Electron*, **89**, 1031-1036 (2006).
4. T.Mizutani, M.Ito, S.Kishimoto, and F.Nakamura, *IEEE Electron Device Letters*, **28**(7), 549-551 (2007).
5. W. Huang, T. P. Chow, Y. Niiyama, T.Nomura, T.Yoshida, *IEEE Electron Device Letters*, **30**(10), 1018-1020 (2009).
6. H. Otake, S. Egami, H. Ohta, Y. Nanashi, and H. Takasu, *Japanese Applied Physical Letter*, **46**, L599-L601 (2007).
7. W. Saito, Y. Tanaka, M. Kuraguchi, K. Tsuda, and I. Ohmura, *IEEE Trans. Electron Device*, **53**(2), 356-362 (2006).
8. W. B. Lanford, T. Tanaka, Y. Otoki, and I. Adesida, *Electron Letter*, **41**, 449-450 (2005).
9. Y. Niiyama, T. Shinagawa, S. Ootomo, H. Kambayashi, T. Nomura, and S. Kato, *Furukawa Review*, **36**, 1-5 (2009).
10. K. Matocha, T. P. Chow, and R. J Gutmann, *IEEE Electron Devices*, **52**, 6-10 (2005).