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# SPACE-CHARGE-LIMITED CURRENT IN SILICON

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**Abstract**—A simple model embracing single and double injection SCL current in solids is described and a simple quantitative analysis is given. Experimental results for electron and hole currents in silicon are presented and support the model. Square-law dependence of single injection current upon voltage is obeyed within an accuracy of $\pm 0{\cdot}1$ per cent of full scale for small voltages such that the average applied field strength does not exceed about $10^3$ V/cm. Current in excess of the ideal square-law, often by several orders of magnitude, can occur and is interpreted in terms of double injection mechanisms.

**Résumé**—Un modèle simple comprenant l'injection simple et double du courant SCL (à charge d'espace limitée) dans les solides est décrit ici et une analyse quantitative est donnée. Les résultats expérimentaux pour les courants de trous et d'électrons dans le silicium sont présentés et prouvent le modèle. La dépendance à règle carrée du courant d'injection en fonction de la tension est suivie avec une precision de $\pm 1$ pour cent de l'échelle totale pour de petites tensions de sorte que la force de champ moyenne est inférieure à $10^3$ V/cm. Le courant, excédant par plusieurs ordres de grandeurs les valeurs prédites par la règle carrée idéale, peut se produire et est interprété en fonction des termes de mécanismes à double injection.

**Zusammenfassung**—Ein einfaches Modell für raumladungsbegrenzten Stromtransport in Festkörpern wird beschrieben. Es umfasst einfache und zweifache Injektion. Anhand dieses Modells wird eine quantitative Analyse der zu erwartenden Stromspannungskennlinie gegeben. Experimentelle Ergebnisse für Elektronen- und Löcherströme in Silizium stehen mit der Modellvorstellung im Einklang. Bei einfacher Injektion wird eine quadratische Abhängigkeit des Stromes von der Spannung mit einer Genauigkeit von $\pm 0{,}1\,\%$ bezogen auf Vollausschlag beobachtet. Allerdings nur für kleine Spannungen, die eine mittlere Feldstärke von höchstens $10^3$ V/cm ergeben. Der Strom kann die ideale quadratische Abhängigkeit überschreiten, oft um mehrere Grössenordnungen. Dieser Effekt wird mit Hilfe von zweifacher Injektion erklärt.

## INTRODUCTION

IN ORDER to achieve space-charge-limited (SCL) current in a solid the dielectric relaxation time of the material used must be long compared with the transit time of the charge carriers. This condition can be achieved without difficulty in materials such as cadmium sulphide, which have a very high intrinsic resistivity. The square-law characteristic described by MOTT and GURNEY[1] for steady SCL current in solids was first observed by WRIGHT[2] in this material following the observation of transient currents by SMITH and ROSE.[3] Single crystal silicon is now available however of sufficiently high purity and resistivity that SCL behaviour can be observed using electrode spacings which are representative of those employed in semiconductor device technology. Silicon is chemically and physically stable, is available in pure single crystal form, has a well understood and reliable technology, and occupies a dominant place in semiconductor device manufacture. It has been pointed out[4] that it is therefore very suitable for the study and exploitation of SCL current in solids.

Injection currents in *p*-type silicon have been observed by GREGORY and JORDAN[5,6] at temperatures ranging from 4·2 to 300°K. At low temperatures, with compensated high resistivity material current was predominantly trap-controlled. At the higher temperatures, using material of lower

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resistivity, trapping effects were absent but ohmic currents were comparable to or larger than the injection currents. SCL current in *p*-type silicon has been reported also by OKAZAKI and HIRAMATSU.[7] A series of measurements with *n*-type diodes has been reported by DENDA and NICOLET[8] who observed square-law behaviour at low applied voltages tending to a three-halves power law at large applied voltages. These results were interpreted in terms of field dependence of carrier mobility as described by LAMPERT.[9] Transient SCL currents in silicon have been studied by LEMKE[10] and have been used to investigate capture cross-sections of iron and gold centres in silicon.

Device exploitation of space-charge current in solids has developed slowly but is now established. Thus square-law silicon diodes have been demonstrated by BÜGET and WRIGHT[11] and are suitable for such applications as power and r.m.s. measurement, analogue multiplication, amplitude compression and expansion, modulation, gain control and function generation. The space-charge transit time oscillator has been described by READ[12] and is now being developed as a high-frequency power source. The space-charge varactor, in which switching from one constant value of capacitance to another takes place rapidly as the applied voltage polarity through a range of a few times $kT/e$, has been described by WRIGHT[13] and by HOWSON *et al.*[14] The surface-channel triode (MOST), which may ultimately form the basis of microelectronics, is fundamentally a space-charge-limited device because the lines of flux from the control electrodes terminate on injected mobile space-charge in the conducting channel of the device.[15] Development of the heterojunction transistor with space-charge-limited emitter, as described by WRIGHT[16] and by BROJDO *et al.*[17], offers in theory the most promising approach for achievement of a microwave solid-state triode.

## EXPERIMENTAL

In this paper the fabrication of experimental silicon diodes is described. Experimental results for single and double injection currents are presented and interpreted.

Diodes were constructed from high purity silicon of resistivity about 25,000 Ω-cm. The starting material was in the form of thin slices about 10-thou. thick cut in (111) orientation. These were diced into 3-mm squares and etched in 19 : 1 mixture of nitric acid and hydrofluoric acid to a final thickness usually between 10 and 20 $\mu$. Injecting contacts were applied over the whole of one surface using evaporated aluminium followed by alloying for hole injection (*p*-type diodes) and using evaporated gold–antimony followed by alloying or electroless nickel plate followed by sintering for electron injection (*n*-type diodes). In all cases the collecting contact (drain) was an evaporated gold layer and was used to define the effective area of the diode. All evaporation, alloying and sintering processes were carried out in vacuum of order $10^{-5}$ mm Hg.

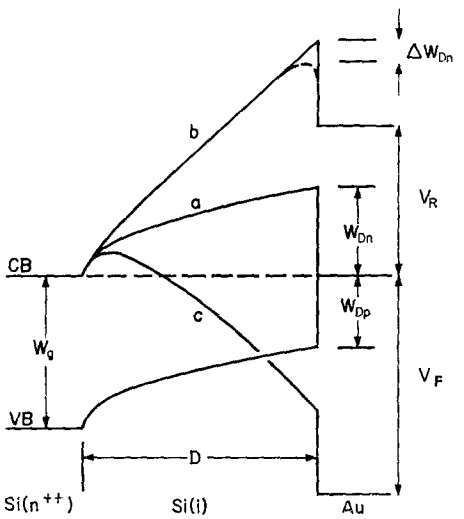


FIG. 1. Energy band configuration for SCL silicon diode. Curve (*a*) is for zero current equilibrium, curve (*b*) represents reverse bias and curve (*c*) represents forward bias. The source to drain spacing is *D*.

## I-V CHARACTERISTICS

### *Theory*

The energy band configuration of the diode is shown in Fig. 1. This is drawn specifically for the case when electrons are the charge carriers but a similar diagram obtains of course when holes are the charge carriers. The injecting contact (source) is shown as $n^{++}$ material and the drain contact is shown as an abrupt potential energy discontinuity. These are considered to be the practical conditions existing.

Because the energy band gap of silicon is relatively small it is possible for significant thermionic

emission of carriers to take place over the drain potential step from the metal contact into the silicon. When the source is electron injecting, for example, this will result in hole injection at the drain under conditions of forward bias. Thus forward current is due to carriers of both signs.

When current is carried by both positive and negative carriers we have

$$J_n = e\mu_n nE \tag{1}$$

$$J_p = e\mu_p pE \tag{2}$$

$$J_F = J_n + J_p. \tag{3}$$

In these equations carrier diffusion has been neglected. This is justified by the detailed analysis of one-carrier current given by WRIGHT[18] which shows that the main effect of diffusion is creation of a virtual source at the injecting contact and that elsewhere its effects are small.

The divergence of electric field is given by the difference between the injected electron and hole densities. Thus

$$\frac{dE}{dx} = -\frac{e(n-p)}{\epsilon}. \tag{4}$$

In these equations carrier generation and trapping have been neglected. This is not wholly justified for even in material of the purity used there are sufficient residual impurities to produce observable effects in thick diodes at small applied voltages. However, by using thin crystal wafers, of the order 10–20 $\mu$ thick, it is possible to reduce such effects to very small proportions. Carrier generation and trapping are therefore neglected in this simple analysis.

At the low current densities and short carrier transit times representative of operation under SCL conditions hole–electron recombination is negligible and the divergence of both hole and electron current is zero. Thus

$$\frac{dJ_n}{dx} = \frac{dJ_p}{dx} = \frac{dJ_F}{dx} = 0. \tag{5}$$

From equations (1), (2) and (5) it can be seen that at a given current density the ratio of electron to hole density is the same at all points in the crystal. Thus

$$\frac{p}{n} = \frac{\mu_n J_p}{\mu_p J_n} = \beta. \tag{6}$$

Substitution for $p$ in equations (1)–(4) and integration with the usual boundary conditions that $n = \infty$ and $E = 0$ at $x = 0$ gives the results

$$E = -\left[-\frac{2J_F x(1-\beta)}{\epsilon(\mu_n+\beta\mu_p)}\right]^{1/2} \tag{7}$$

$$n = \frac{1}{e}\left[-\frac{\epsilon J_F}{2x(1-\beta)(\mu_n+\beta\mu_p)}\right]^{1/2} \tag{8}$$

$$V = \frac{2}{3}\left[-\frac{2J_F(1-\beta)}{\epsilon(\mu_n+\beta\mu_p)}\right]^{1/2} x^{2/3}. \tag{9}$$

The negative signs inside the square-roots in these equations arise from the fact that current density $J_F$ is algebraically negative. From these equations we have in particular that

$$-J_F = \frac{9\epsilon}{8}\frac{(\mu_n+\beta\mu_p)}{(1-\beta)}\frac{V_F^2}{D^3}. \tag{10}$$

In this equation $V_F$ is the applied drain forward voltage and $D$ is the source to drain spacing. In these various equations the quantity $\beta$ is, as yet, undetermined. Its value can be found however, by consideration of conditions at the drain contact. At small applied voltages current is small and it is justified to regard the hole density at the drain as being in thermal equilibrium with the drain metal. Thus $p_D = N_v \exp(-W_{Dp}/kT)$ and from equations (6) and (8) we have

$$\beta = \frac{4ep_D D^2}{3\epsilon V_D + 4ep_D D^2}. \tag{11}$$

Substitution in equation (10) gives the result

$$-J_F = \frac{3ep_D(\mu_n+\mu_p)V_F}{2D} + \frac{9\epsilon\mu_n V_F^2}{8D^3}. \tag{12}$$

At large applied voltages the hole current across the drain contact will saturate at the value $J_{ps}$ given by the Richardson thermionic emission equation. In this case we have from equations (3) and (6) that

$$\beta = \frac{\mu_n J_{ps}}{\mu_p(J_F - J_{ps})}. \tag{13}$$

Substitution in equation (10) gives the result

$$-J_F = \left[1+\frac{\mu_n}{\mu_p}\right]J_{ps} + \frac{9\epsilon\mu_n V_F^2}{8D^3}. \tag{14}$$

If $p_D$ and $J_{ps}$ are sufficiently small each of equations (12) and (14) reduces to the standard Mott–Gurney law. This situation occurs when the drain potential step $W_{Dp}$ is large. Conditions then reduce to the one-carrier case and we have

$$-J_F = \frac{9\epsilon\mu_n V_F^2}{8D^3}. \tag{15}$$

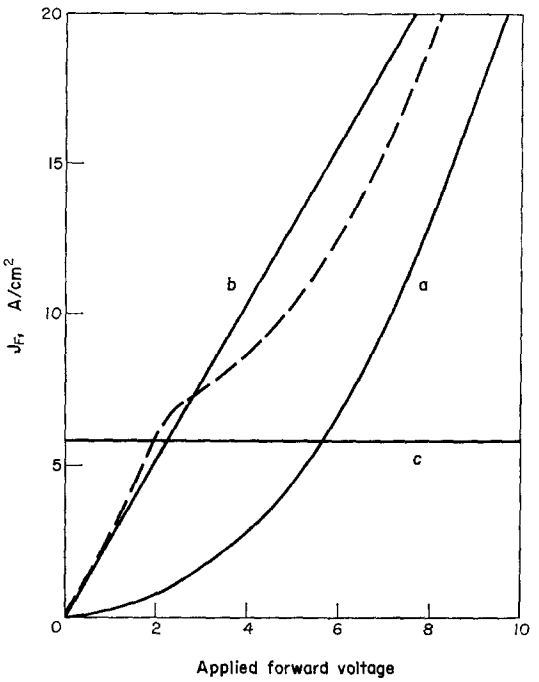


FIG. 2. Representative forward current characteristics calculated for SCL silicon diode. Source to drain spacing: $D = 20\ \mu$. Drain potential step for holes: $W_{Dp} = 0{\cdot}375$ eV. Curve (*a*) is the ideal Mott–Gurney square-law of equation (15). Curve (*b*) is the linear current term of equation (12). Curve (*c*) is the saturation current term of equation (14). The broken line curve shows the resultant I–V characteristic which is observed in this case.

In all these equations $V_F$ represents the "inner" potential difference measured within the crystal from virtual source to drain. It is related to the external applied voltage by the equation

$$V_F = V_A - V_0 \tag{16}$$

where $V_0$ is a threshold voltage for current. $V_0$ is determined basically by the difference between the magnitudes of the drain potential step and the potential maximum at the virtual source.

Equations (12), (14) and (15) are illustrated in Fig. 2. Typical values for device dimensions have been used with the value of 0·375 eV for $W_{Dp}$ and the value of $5 \times 10^6$ cm/sec for the thermal velocity of holes crossing the drain contact. These values are somewhat arbitrary but are representative figures suitable for purposes of illustration.

It is clear that depending on the relative magnitudes of the various terms involved in these equations a variety of current characteristics may be expected.

*Experimental*

Steady current characteristics for both forward and reverse bias were measured point by point using standard multi-meters. Reverse current measurements will be discussed first as these are relatively straightforward to interpret. Further, they provide information about the nature of the drain contact to assist interpretation of forward current measurements.

*Reverse current.* For the diode using electrons reverse bias conditions exist when the drain is made negative with respect to the source. This is curve (*b*) of Fig. 1. Under these conditions current is carried wholly by thermionic emission of electrons from the drain contact into the silicon. Current is therefore described by the Richardson equation for a potential step $W_{Dn}$ modified by image force lowering of amount $\Delta W_{Dn}$. Thus

$$J_R = kT^2 \exp\left(-\frac{eW_{Dn}}{kT}\right) \exp\left(\frac{e\Delta W_{Dn}}{kT}\right) \tag{17}$$

where

$$\Delta W_{Dn} = \frac{e^{3/2}E_D^{1/2}}{2\pi^{1/2}\epsilon^{1/2}}. \tag{18}$$

In this latter equation the field $E_D$ is that existing at the drain contact. With sufficient accuracy for the large applied voltages for which this term is significant it may be set equal to $V_F/D$.

Equation (17) is valid for applied voltages greater than several times $kT/e$ for which saturation of thermionic emission occurs. Thereafter current increases slowly as the image forces gradually reduce the barrier height. A typical set of reverse current characteristics is shown in Fig. 3. These follow equation (17) very well.

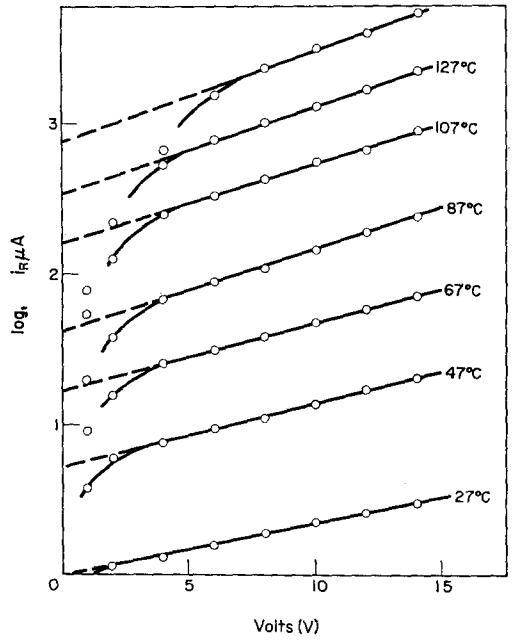


FIG. 3. Reverse current characteristics measured for $n$-type silicon diode at various temperatures.

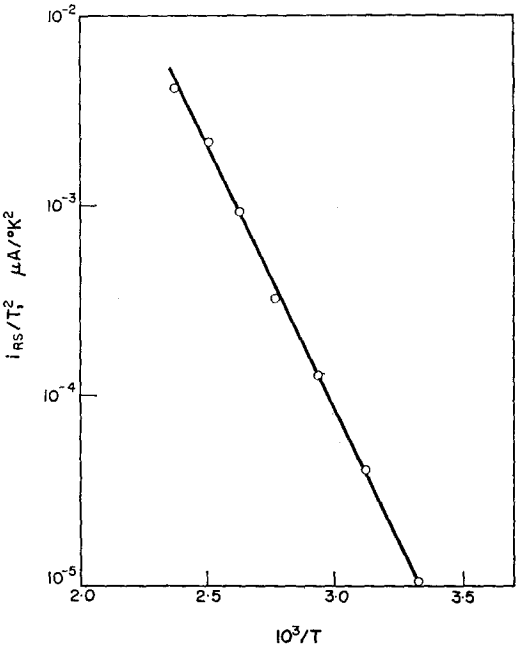


FIG. 4. Richardson plot for the diode of Fig. 3.

From curves of the sort shown in Fig. 3 it is possible to obtain a fairly good estimate of $W_{Dn}$. Extrapolation of each curve to zero voltage gives $J_{Rs}$, the thermionic saturation current crossing the drain contact. A plot of the quantity log $(J_{RS}T/^2)$ against $1/kT$ is linear and has slope $-eW_{Dn}$. Thus the value of $W_{Dn}$ may be obtained. This analysis is illustrated by Fig. 4 which shows a plot of this kind derived from the measurements shown in Fig. 3. Measurements of this kind were carried out on many diodes and the results are summarized in Table 1.

*Table* 1. *Potential energy step for thermionic emission of carriers from gold to silicon*

| Diode type | $W_{Dp}$, eV | Diode type | $W_{Dn}$, eV |
|---|---|---|---|
| $p$ | 0·53 | $n$ | 0·59 |
| $p$ | 0·56 | $n$ | 0·52 |
| $p$ | 0·62 | $n$ | 0·61 |
| $p$ | 0·46 | $n$ | 0·62 |
| $p$ | 0·61 | $n$ | 0·51 |
| $p$ | 0·38 | $n$ | 0·58 |
| $p$ | 0·44 | $n$ | 0·57 |
| $p$ | 0·41 | $n$ | 0·46 |
| $p$ | 0·59 | $n$ | 0·69 |
| $p$ | 0·68 | $n$ | 0·53 |
| $p$ | 0·52 | $n$ | 0·70 |
| | | $n$ | 0·41 |
| Mean $W_{Dp}$ | 0·53 | Mean $W_{Dn}$ | 0·57 |

The measurements given in this Table demonstrate, first, the considerable scatter which occurs in contact potential step even when contacts are fabricated under what are ostensibly identical conditions. Variations of up to 0·3 eV were observed, sufficient to cause several orders of magnitude variation in current. Such effects are not unexpected of course in view of the sensitivity of work function to surface impurities on an atomic scale. The most likely form of impurity is oxide layers which form very rapidly on silicon. Charges trapped in such layers are known to cause significant changes in work function even when the layers are very thin, of the order of a few atomic thicknesses. Second, it is satisfactory to note that the average values of $W_{Dp}(\bar{W}_{Dp} = 0{\cdot}53$ eV) and $W_{Dn}(\bar{W}_{Dn} = 0{\cdot}57$ eV) add up to 1·10 eV. This compares very well with the value of 1·12 eV for

the thermal band gap of silicon at 300°K. This implies that the interpretation of the reverse current characteristics is substantially correct and justifies the energy band configuration given in Fig. 1. Third, the value of 0·57 eV for $\bar{W}_{Dn}$ differs from the value of 0·8 eV which is given as the difference between the thermionic work function of gold ($\phi_{Au} = 4{\cdot}8$ eV) and the electron affinity of silicon ($\chi_{Si} = 4{\cdot}0$ eV). The difference of rather more than 0·2 eV is probably accounted for partially by small experimental errors but for the most part by the fact that the work function of an evaporated layer is not necessarily the same as that of the bulk material. Also, if oxide layers are present, the formation of dipole layers across the silicon–oxide–gold interface will affect the contact potential difference. The strengths of such dipole layers would vary in a random manner between different experimental runs, depending for instance on the thickness of the oxide layer, so that random variations in $W_D$ would occur, as observed, from this cause if from no other.

*Forward current.* The simple theory outlined previously indicates that a variety of forward current characteristics may be expected depending on the position of the Fermi-level of the drain contact metal with respect to the mid-band-gap level of the silicon. In particular, if the Fermi-level of the drain metal lies near to the silicon mid-band-gap level good rectifying diodes should be obtained in which forward current is one-carrier and follows the Mott–Gurney square-law dependence on applied voltage. A small number of the diodes constructed showed these properties and were selected for further study of one-carrier SCL current.

Figures 5 and 6 show two typical sets of measurements on single injection diodes. These refer to electron and to hole diodes respectively. In each case it can be seen that the Mott–Gurney square-law is obeyed accurately over the ranges of voltages and temperature used.

The temperature dependence of SCL current is caused by changes in the threshold, or offset, voltage $V_0$ and by changes in carrier mobility. The offset voltage is a measure of the difference between the contact potential step and the potential hump at the virtual source. The latter increases as temperature rises so the offset voltage decreases. This effect is relatively small. The most important

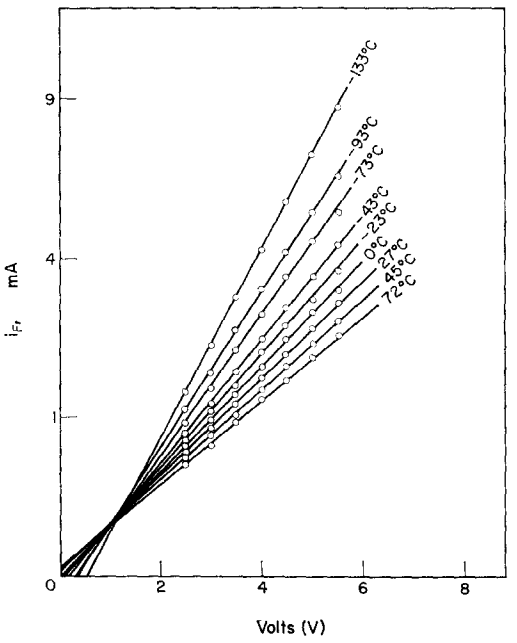


FIG. 5. Forward current characteristics of *n*-type silicon diode at various temperatures. Source to drain spacing: $D = 28\mu$. Source area $A = 0{\cdot}48$ mm².

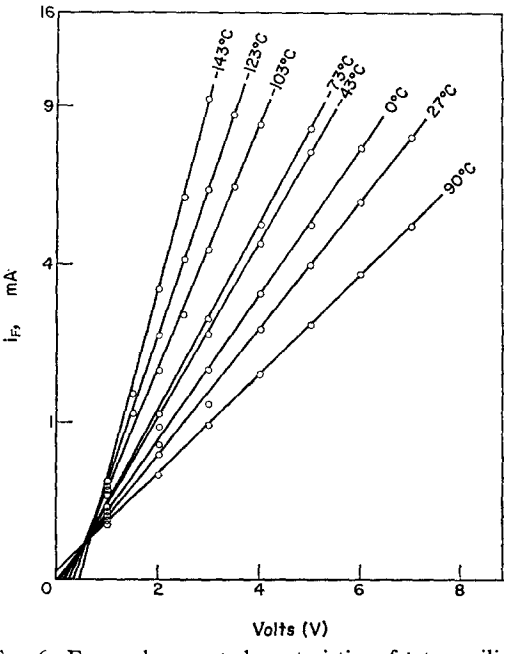


FIG. 6. Forward current characteristics of *p*-type silicon diode at various temperatures. Source to drain spacing: $D = 38\ \mu$. Source area $A = 1{\cdot}5$ mm².

factor controlling the temperature dependence of current is carrier mobility. From the slopes of the curves shown in Figs. 5 and 6 the perveance $P$ of the diodes may be obtained. This quantity is directly proportional to carrier mobility and its temperature dependence may be compared with the temperature dependence of mobility $\mu_H$ derived from Hall effect measurements. This can be done conveniently be evaluating the ratio $P/\mu_H$ as a function of temperature. In all cases, for both $n$-type and $p$-type diodes this ratio was found to be constant over the temperature range used from about $-150$ to about $+90$°C, confirming that the temperature dependence of perveance is due only to temperature dependence of carrier mobility. It is relevant to point out here that this series of measurements confirms that carrier trapping is negligible as expected. If this was not so then the ratio $P/\mu_H$ would decrease rapidly as temperature decreased and trapping became more effective.

Precision measurements, using digital voltmeters, were made on a number of $p$-type diodes to assess the accuracy of the square-law response. Diodes for these measurements were selected to have $V_0$ as small as possible. This occurs in diodes in which the drain contact potential step is just balanced by the potential hump at the virtual source. During the measurements diodes were immersed in ice baths to maintain constant temperature conditions. It was found that current followed a square-law dependence upon applied voltage within an accuracy of $\pm 0{\cdot}1$ per cent of full-scale with respect to voltage providing that the mean field strength across the device did not exceed about $10^3$ V/cm. For a diode with an electrode spacing of 50 $\mu$ for example this means that the square-law response is accurate within 0·1 per cent for applied voltages up to about 5 V. The decrease of current at larger voltages is attributed to field decrease of mobility which makes the I–V characteristic tend towards a three-halves power law as described by Lampert and as observed by Denda and Nicolet. For small departures from the low field value we may write $\Delta\mu = -\alpha E^2$ where $\alpha$ is a coefficient depending on the type of carrier, the temperature, and the particular scattering mechanism involved. It is best regarded as a quantity to be determined experimentally by measuring the decrease of perveance at large applied voltages. Providing that the decrease of mobility is small it is sufficiently accurate to average the mobility across the diode to obtain

$$J = \frac{9\epsilon\mu}{8}\left[1 - \frac{9\alpha V_F^2}{8D^2}\right]\frac{V_F^2}{D^3}. \qquad (19)$$

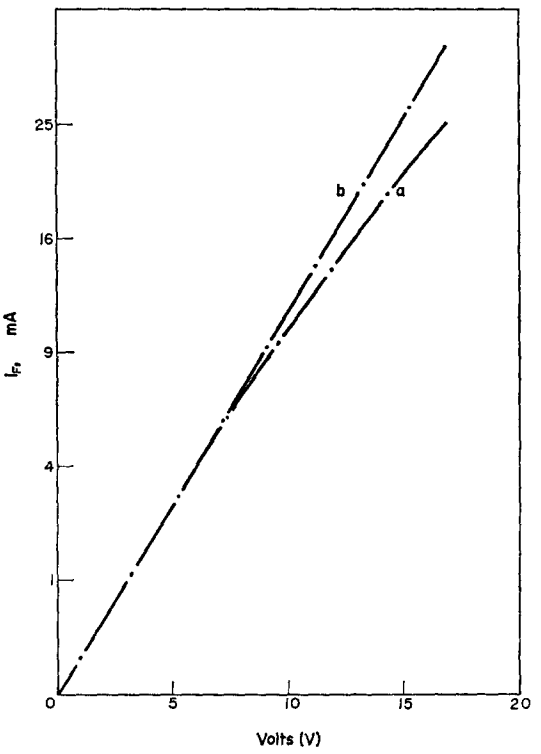


FIG. 7. Forward current characteristic of $p$-type diode, measured at 0°C, showing accuracy of square-law at small applied voltages and the deviation from the square-law at large applied voltages caused by field decrease of hole mobility. Source to drain spacing: $D = 50\,\mu$. Source area $A = 2{\cdot}8$ mm$^2$. Curve ($a$): measured characteristic at 0°C. Curve ($b$): measured characteristic corrected for quadratic field decrease of mobility using the value $\alpha = 2\times10^{-12}$ m$^2$ V$^{-2}$.

A typical set of high precision measurements is shown in Fig. 7. The measured values are fitted very well by equation (19) with $\alpha = 2\times10^{-12}$ m$^2$V$^{-2}$ providing that the decrease of mobility is less than about 10 per cent. It is of interest to note that, as for germanium, this measured value is considerably less than the value $\alpha = 3\pi\mu^2/64u^2$, where $\mu$ is the low field mobility and $u$ is the longitudinal acoustic wave velocity, given by simple

theory. Equation (19) is valid therefore up to mean field strengths of about $3 \times 10^3$V/cm. For a diode of thickness $50\mu$ this corresponds to an applied voltage range from 0 to 15 V.

When the thermionic emission current of carriers of opposite kind entering from the drain contact becomes comparable with the one-carrier current drawn from the source contact, double injection behaviour should be observable as described by equations (12) and (14). I–V characteristics of the type illustrated by Fig. 2 were in fact observed in many diodes. A representative set of oscillographs for $p$-type diodes is shown in Fig. 8 to demonstrate this. Curve (*a*) shows the ideal Mott–Gurney square-law response. Curve (*b*) applies to the situation in which the drain Fermi-level has moved towards the silicon conduction band by about 0·1 eV from the mid-band-gap level. In this case current increases at small voltages as described by equation (12). At a current of about 1 mA however the thermionic emission of electrons from the drain saturates and current thereafter follows equation (14). The position of the "knee" is very sensitive to temperature. By cooling sufficiently it can be eliminated. Curve (*c*) applies to the situation in which the drain Fermi-level is not far from the conduction band edge so that copious thermionic emission of electrons occurs into the silicon at this contact. In this case the first term of equation (12) is predominant. Current rises very steeply, almost linearly, and can be several orders of magnitude greater than the one-carrier current. The physical reason for this is of course that space-charge neutralization is almost complete so that although a high density of mobile charge exists in the diode the voltage developed is small. Under these circumstances high current densities can exist at small applied voltages.

The threshold, or offset, voltage which can be observed in these oscillographs originates from the same causes as for the measurements shown in Figs. 5 and 6.

The diode characteristics shown in the oscillographs of Fig. 8 all refer to different devices. However, it is possible to achieve all of these characteristics successively in the same device by repeated removal of the existing drain contact (by etch, for instance) and evaporation of another. The new evaporated layer usually has a different work function from that of the layer preceding it and the I–V characteristic of the diode is often modified considerably. Thus by removal and re-application of the drain contact it is possible to convert diodes of types (*b*) and (*c*) into type (*a*), showing the ideal Mott–Gurney square-law and vice-versa. The fact that this can be done supports the supposition that a double-injection mechanism is involved in diodes which show current in excess of the Mott–Gurney law.

If the Fermi-level of the drain contact lies very near to the conduction band edge the drain becomes, in effect, a fully injecting contact. Under these circumstances it is not possible for either electrons or holes to be the majority carrier over the whole region from source to drain. The ratio of electron to hole density can, then, no longer be the same at all points in the crystal and the analysis given previously is not valid. In this situation of full double-injection it is necessary to take into account both carrier diffusion and carrier recombination. Detailed discussions of this situation have been given, for example, by LAMPERT and ROSE,[19] LARRABEE[20] and BARON.[21] The present experiments did not include this case and it will not be further discussed.

## C–V CHARACTERISTICS

Measurements of incremental capacitance were made for forward and reverse bias voltages.

### *Reverse bias*

In silicon of 25,000 Ω-cm resistivity the Schottky depletion layer at 1 V applied is about 100 $\mu$ thick. This is much greater than the electrode spacings used. Consequently the reverse bias capacitance is expected to be independent of voltage bias and equal to the geometrical capacitance. This was observed.

### *Forward bias*

The forward bias capacitance contains three components. The first of these is the geometrical capacitance of the electrodes and is numerically equal to the reverse bias capacitance. The second is the "electronic" capacitance originating in the finite transit time of the charge carriers across the diode. This capacitance has been discussed by SHAO and WRIGHT;[22] it is negative in nature and is numerically equal to one-quarter of the geometrical capacitance. The third component is surface-

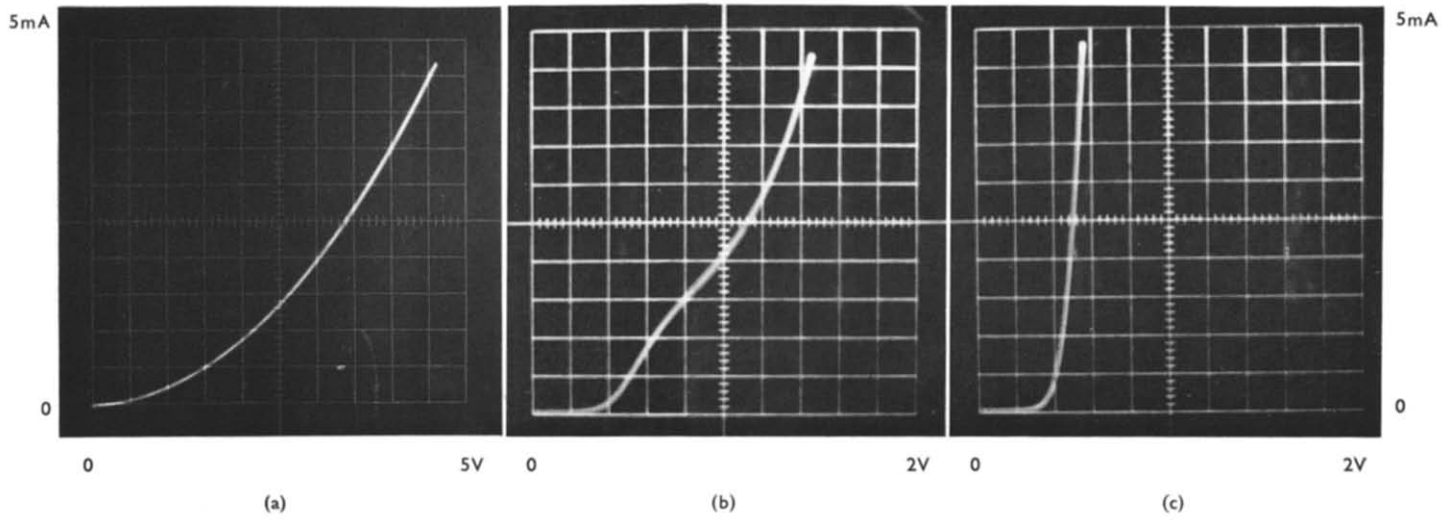


FIG. 8. Forward current characteristics for single and double injection diodes.

Oscillogram (*a*) Single injection current showing Mott–Gurney square-law. Drain emission negligible.

Oscillogram (*b*) Double injection current showing "knee" as saturation of drain emission sets in (see Fig. 2).

Oscillogram (*c*) Double injection current with large drain emission. Current described predominantly by first term of equation (12).

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states capacitance at the drain interface. This is readily seen under SCL conditions for in thick diodes current densities are low and the charge "stored" in the conducting channel of the diode is small compared with the charge trapped in surface states. Surface-states effects can be avoided by making measurements at high frequencies at which the trapped charges cannot respond. Measurements made at frequencies above about 1 Mc/s showed a forward bias capacitance independent of bias, and approximately equal to three-quarters of the geometrical capacitance as expected.

## CONCLUSIONS

A simple theoretical model embracing single and double injection SCL current in solids has been described and analysed. Experimental results for electron and hole currents in silicon have been presented. These are consistent and show that the simple theoretical model adopted is adequate for the interpretation of experimental data. In particular the square-law dependence of current upon voltage for single injection current is followed very accurately for small applied voltages ($E_{av} < 10^3$ V/cm). At larger applied voltages ($E_{av} > 10^3$ V/cm) deviations from the ideal square law occur because of field decrease of carrier mobility. Currents in excess of the ideal square-law behaviour, often by several orders of magnitude, occur frequently and can be explained in terms of double injection mechanisms.

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