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InAs-Channel Metal-Oxide-Semiconductor HEMTs with Atomic-Layer-Deposited Al_2O_3 Gate Dielectric

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N-type metal-oxide-semiconductor high electron mobility transistor (MOS-HEMT) devices with an InAs-channel using atomic-layer-deposited (ALD) Al_2O_3 as a gate dielectric have been fabricated and characterized. The device performances of a set of scaled transistors with and without high-*k* gate dielectric Al_2O_3 have been compared to determine the optimum device structure for low power and high speed applications. The measurement results revealed that the high performance InAs-channel MOS-HEMTs with the ALD Al_2O_3 gate dielectric can be achieved if the structure is designed properly.
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To further integrate with a Si complementary metal oxide semiconductor (CMOS) and to extend a CMOS front-end technique to 22 nm and beyond, planar III-V compound semiconductor field-effect transistors (FETs) have been identified as one of the most attractive devices for nanoelectronic applications.[1-3] Intel Corporation proposed benchmarking techniques to gauge the progress of such nanotechnology researches for high performance and low power logic applications against the best Si metal-oxide-semiconductor field-effect transistor (MOSFET) data.[4] The excellent radio-frequency (rf) performance has been demonstrated by InAlAs/InGaAs high electron mobility transistors (HEMTs) on an InP or GaAs substrate.[5,6] A higher electron mobility and velocity can be realized by the increase of the indium content in the InGaAs channel, which makes InAs-channel heterostructure field-effect transistors (HFETs) well suitable for low power and high speed logic applications because of the extremely high electron mobility of more than 3000 cm^2/V s.[7] Despite all the excellent performances, the implementation of high-κ insulating gate dielectrics to further reduce the gate leakage current for performance improvement is inevitable to meet the future requirements of International Technology Roadmap for Semiconductors.

Recently, research efforts on the atomic-layer-deposited (ALD) growth of Al_2O_3 on III-V compound materials attracted particular attention since other familiar ALD HF-based dielectrics have been widely used in the Si industry.[3,8,9] Because of its excellent dielectric properties with high thermal and chemical stabilities, Al_2O_3 is widely used as a gate dielectric and a tunneling barrier and for surface passivation. Al_2O_3 shows a high bandgap (~9 eV), a high breakdown electric field (5–30 MV/cm), and a high thermal stability (over 850°C).[3] A high performance Al_2O_3/InGaAs MOSFET has been proposed and demonstrated with excellent dc performance.[3] For logic applications, the Al_2O_3/InGaAs MOSFET was also benchmarked with scaling metrics, such as a current on/off ratio, a subthreshold slope, and a drain-induced barrier lowering, and showed a high potential as a candidate for integration in a Si platform.[10]

Our previous work successfully demonstrated a high speed, low power consumption, and low noise InAs-channel devices with an 80 nm gate length.[11,12] In this article, the ALD high-κ dielectric Al_2O_3 films deposited on an InP etch-stop layer of InAs-channel HEMTs for metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs) are fabricated and evaluated. The main focus is on the evaluation of such devices for ultralow power rf applications to study the feasibility of a possible integration of both digital and rf applications on the same platform.

Experimental

The MOS-HEMT structure was grown on a 2 in. semi-insulating InP substrate by molecular beam epitaxy, as shown in Fig. 1. The device isolation was achieved by wet chemical etching. Before the ALD Al_2O_3 gate dielectric deposition, the $In_{0.53}Ga_{0.47}As$ cap layer was selectively etched by wet chemical etching using a succinic-acid-based solution. The cap etching stopped at the InP etching-stop layer due to the high etching selectivity between an $In_{0.53}Ga_{0.47}As$ cap layer and an InP etching-stop layer. Then, the wafer was treated in a diluted HCl solution (1:10) for 60 s, and then the surface was dipped into an ammonium sulfide solution $[(NH_4)_2S_x]$ at 60°C for 25 min. Those treatments were performed to etch the native oxide and to tie up the dangling bonds of the surface. Following the surface cleaning, high quality Al_2O_3 was deposited by atomic layer deposition at 300°C and then annealed at 600°C. Ohmic contact was formed by selectively etching the gate dielectric. Source and drain ohmic metals were formed with 240 nm thick Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250°C for 30 s. In this work, the source–drain spacing for both the regular HEMT and the MOS-HEMTs is 3 μm. The T-shaped gate lithography was carried out in a 50 keV JEOL electron-beam lithography system (E-beam). The Ti/Pt/Au gate metal was deposited by evaporation and lifted off

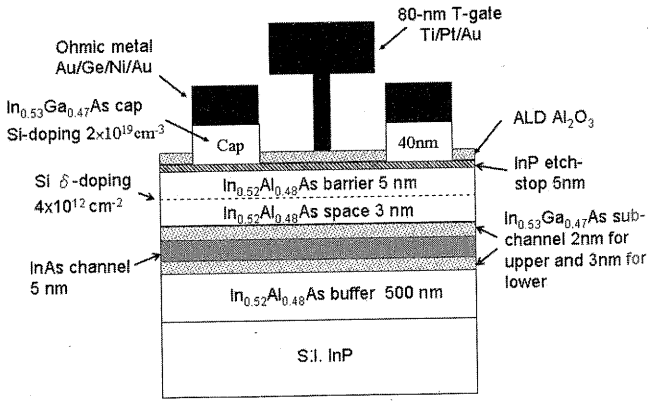

Figure 1. Schematic cross-sectional diagram of an InAs-channel MOS-HEMT with ALD Al_2O_3 gate dielectric.

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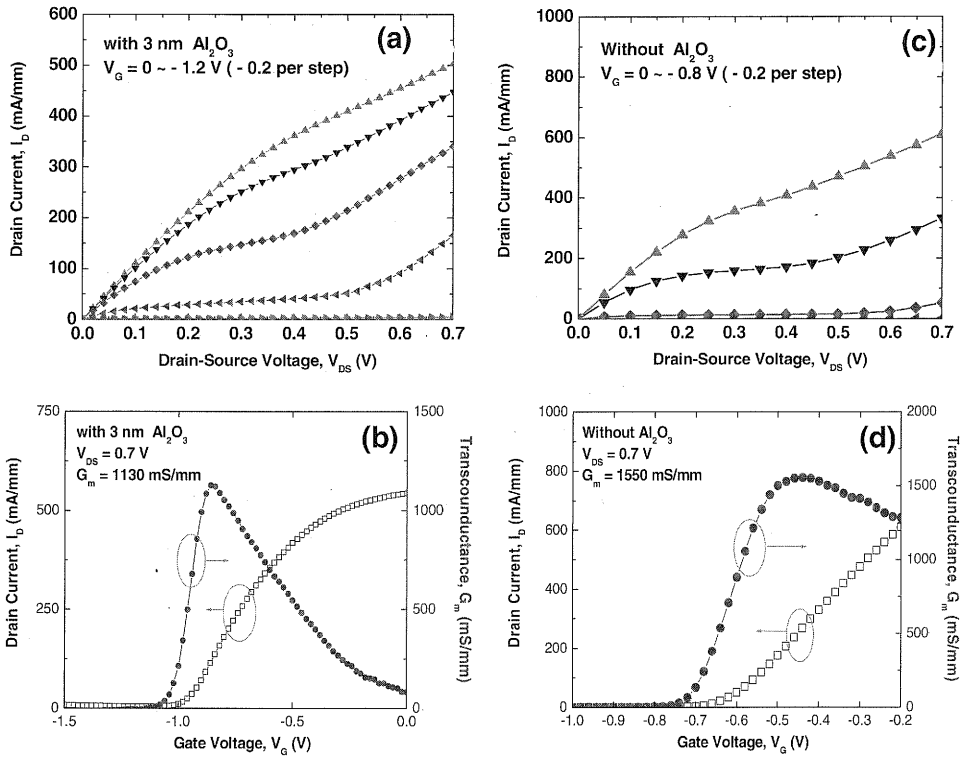

Figure 2. (Color online) (a) Extrinsic drain current and (b) transconductance vs gate bias for an 80 nm InAs-channel MOS-HEMT with 3 nm ALD Al_2O_3 gate dielectric at a V_{DS} of 0.7 V and [(c) and (d)] for InAs-channel HEMT without gate dielectric.

to form the submicrometer T-shaped gate. The gate length of 80 nm was estimated by scanning electron microscopy. For comparison, conventional InAs-channel HEMTs without a high-k dielectric have also been fabricated.

Results and Discussion

The fabricated MOS-HEMTs have a gate length of 80 nm with a high-k dielectric Al_2O_3 thickness of 3 nm. Figure 2a and b shows the dc current–voltage characteristics with a gate bias from 0 to −1.2 V in steps of −0.2 V. As observed from this figure, the MOS-HEMT device can be well pinched off with a threshold voltage of −1.0 V. A maximum drain–source current (I_{DSS}) of 530 mA/mm and a high peak g_m of 1130 mS/mm were obtained for the device at a drain bias of 0.7 V. For comparison, the conventional InAs-channel HEMTs fabricated without an Al_2O_3 high-k dielectric were also characterized at the same V_{DS} bias of 0.7 V, and the results are shown in Fig. 2c and d. The conventional InAs-channel HEMT shows a slightly higher I_{DSS} of 830 mA/mm and a peak g_m of 1550 mS/mm at a V_{DS} bias of 0.7 V. The results indicate that the addition of Al_2O_3 to the HEMT device did not cause much degradation. The InAs-channel MOS-HEMTs still maintained the superior electron transport properties in the InAs channel and demonstrated an excellent dc performance. Furthermore, there is no strong interaction between the high-k dielectric interface and the InAs-channel, and the device operation did not rely on inversion carriers. Figure 3 shows the reduction of the gate leakage current with the use of high-k gate dielectric Al_2O_3. With 7 nm ALD Al_2O_3, the InAs-channel MOS-HEMT shows the smallest gate leakage compared with the conventional one without a high-k dielectric. However, for our specific device with an 80 nm gate length, a thinner than 5 nm gate dielectric is preferred, and the Schottky layer thickness can be further reduced for the optimal aspect ratio to maintain low gate leakage and high speed logic performances simultaneously.

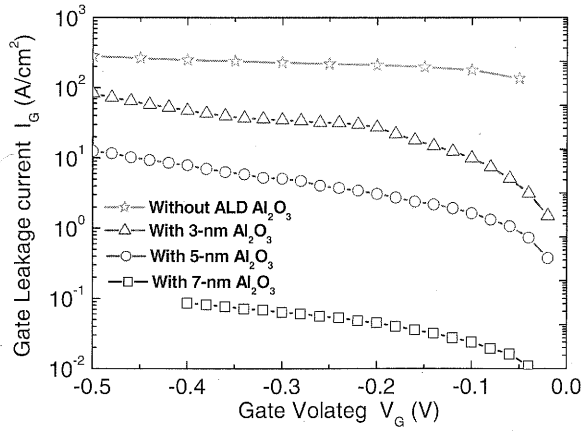

Figure 3. (Color online) Gate leakage current vs voltage for a conventional InAs-channel HEMT and InAs-channel MOS-HEMTs with 3, 5, and 7 nm ALD Al_2O_3 gate dielectrics.

The minimum noise figure and associated gain of the InAs-channel MOS-HEMT from 20 to 60 GHz at V_{DS} of 0.6 V are shown in Fig. 4a. The dc power dissipation was 4.9 mW, and the device demonstrated a typical associated gain of 6 dB with a noise figure of less than 2 dB as measured up to 60 GHz. To compare with the conventional InAs-channel HEMT shown in Fig. 4b, the MOS-HEMT devices show the same noise figure level, but 2 dB lower of the associated gain. Though the MOS-HEMT showed lower transconductance compared to the conventional HEMT due to the increase of the gate-to-channel distance, it still demonstrated excellent dc and rf performance. The InAs-channel MOS-HEMT shows great potential for high speed, ultralow power, and low noise applications.

The S-parameters of a conventional InAs-channel HEMT without a gate dielectric and of an InAs-channel MOS-HEMT with a 3 nm Al_2O_3 gate dielectric were measured using a Cascade Microtech on-wafer probing system with a vector network analyzer from 5 to 80 GHz. A standard load-reflection–reflection-match calibration method was used to calibrate the measurement system. Current gain ($|h_{21}|^2$), Mason's unilateral gain (U_g), and maximum available gain/maximum stable gain (MAG/MSG) as a function of frequency are plotted in Fig. 5. The intrinsic f_T obtained for the InAs-channel

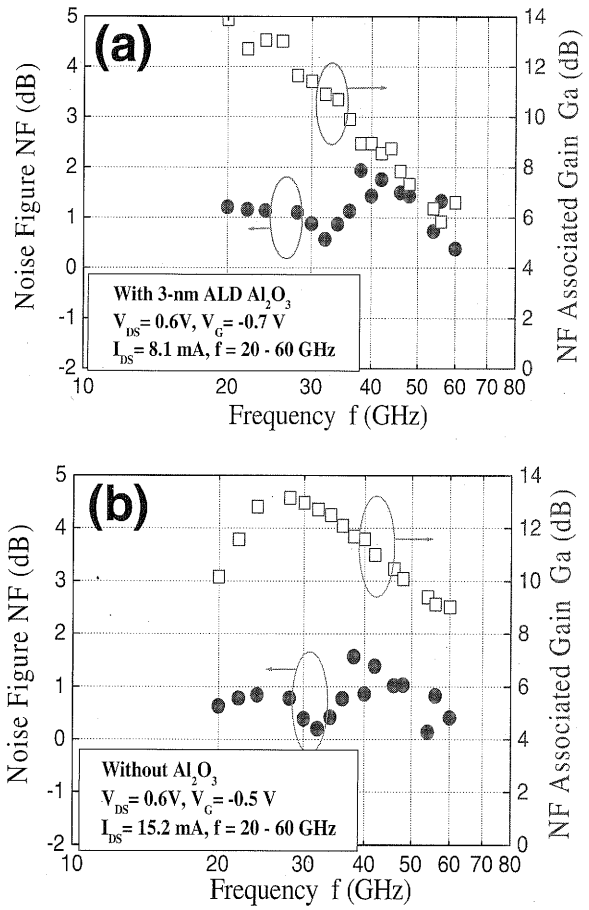

Figure 4. (Color online) Measured minimum noise figure and associated gain (a) for an InAs-channel MOS-HEMT from 20 to 60 GHz at a V_{DS} of 0.6 V with a dc power dissipation of 4.9 mW and (b) for a conventional InAs-channel HEMT at a V_{DS} of 0.6 V with a dc power dissipation of 9 mW.

MOS-HEMT were 185 and 265 GHz at V_{DS} = 0.3 and 0.7 V, respectively. No significant degradation was observed compared to 192 and 330 GHz for a conventional InAs-channel HEMT at the same biases. Such high gain and high frequency response indicate that the high quality of the Al_2O_3/InAlAs interface is achieved, and frequency response is not degraded by the interface trap density (D_{it}).

Conclusions

In this article, we demonstrated 80 nm InAs-channel MOS-HEMTs with high-κ gate dielectric Al_2O_3. With the high-κ gate dielectric, only a small degradation of frequency response was observed. With the high gain and high frequency response, it is indicated that the InAs-channel MOS-HEMTs can be used for high frequency, low noise figure, and low power consumption applications. The superior performance achieved indicated that future integration of digital and rf applications on the same platform could be possible with the optimal device structure.

Acknowledgments

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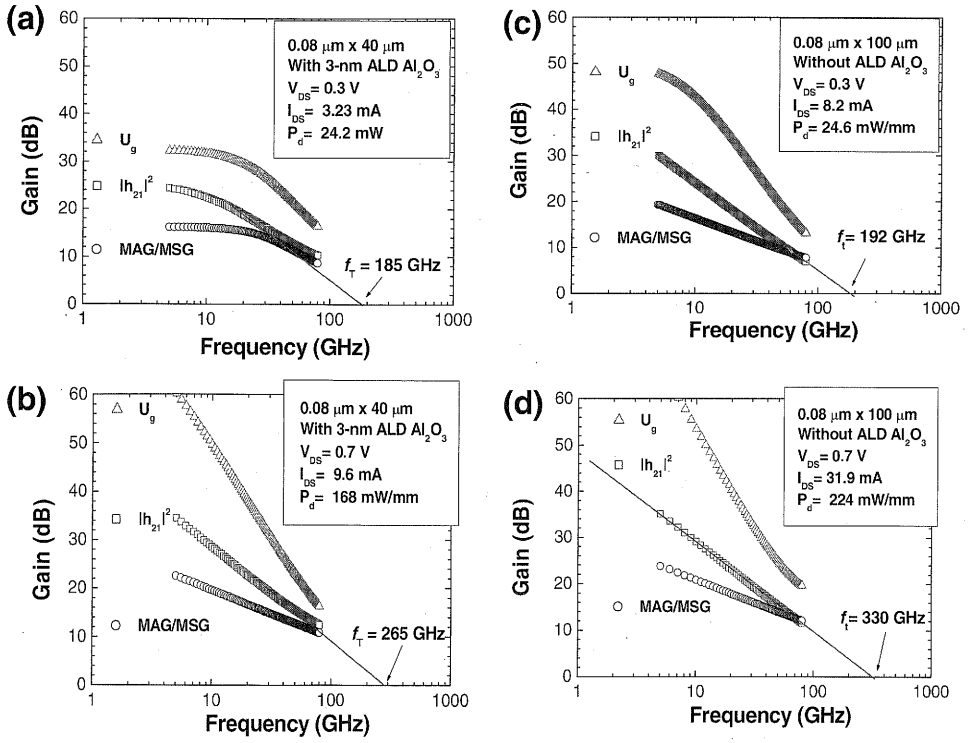

Figure 5. (Color online) Typical current gain $|h_{21}|$, MAG/MSG, and U_g as a function of frequency for an InAs-channel MOS-HEMT with 3 nm ALD Al_2O_3 at a V_{DS} of (a) 0.3 and (b) 0.7 V and for a conventional InAs-channel HEMT without Al_2O_3 at a V_{DS} of (c) 0.3 and (d) 0.7 V, respectively.

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