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A FINITE ELEMENT STUDY OF GEOMETRIC MODIFICATIONS TO REDUCE THERMAL MISMATCH CURVATURE IN WAFER BONDING

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ABSTRACT

Wafer-level packaging of RF MEMS devices offers an attractive option to reduce packaging cost significantly and ensures hermetic encapsulation of devices. Low-temperature cofired ceramic (LTCC) cap wafers are particularly favorable because they can be pre-patterned with through-wafer vias for integrated electrical contacts and high-density packaging, at a much lower cost than silicon wafers with similar features. However, thermal expansion mismatch between ceramic and silicon wafers at high bonding temperatures induces thermal stresses at the interface, resulting in wafer curvature. For example, a 150 mm silicon wafer 675 μm thick with a ceramic cap wafer 500 μm thick has been measured to exhibit out-of-flatness displacement as severe as of 1.7 mm at the center. While the curvature can be reduced significantly using low-thermal-expansion ceramic, such materials are non-standard and require custom formulation. Furthermore, as the wafer diameter is increased, thermal expansion mismatch becomes more problematic. Therefore, it is desirable to address the problem using a geometrical approach in addition to optimizing the ceramic for wafer bonding applications. The present study applies finite element analysis (FEA) to examine the potential for reducing such curvature by introducing slots in the ceramic cap wafer. Two-level factorial design simulations involving five parameters were conducted to investigate the effect of slot parameters on wafer curvature, using 2-D plane strain simulation of wafer cooling from 300 °C to 25 °C. The five parameters investigated were cap wafer thickness, slot width, slot depth, slot separation, and slot orientation. The nonlinear temperature dependence of thermal expansion was also examined based on test data for the ceramic wafers. Furthermore, a 3-D finite element simulation was conducted to compare the 2-D results to overall impact on wafer distortion. FEA results were compared with experimental curvature measurements on sample wafers measured by coordinate measuring machining (CMM). Simulated results suggest that introduction of slots shows reduction in wafer curvature, and the displacement can be reduced by as much as 25% based on the geometric parameter values for slots in the cap wafer.

INTRODUCTION

Microelectromechanical systems (MEMS) have been successfully in many applications including a wide range of sensors for automotive and aerospace industries. However, radio-frequency (RF) MEMS devices, having application in wireless communications, find it difficult to penetrate the highly cost-sensitive market due to technical and economical challenges strongly influenced by packaging. The existence of microscopic moving parts on the devices requires proper sealing from the outside environment and hence both fabrication and packaging of these parts need to be considered simultaneously.

Investigators at Intel Corporation have developed a wafer level packaging method [1] that uses thermo compression bonding (TCB) to bond a low-temperature cofired ceramic (LTCC) cap wafer with metal vias to the MEMS device wafer. The gold metal vias on the cap are pre-filled and provide electrical interconnection with high packaging density. Gold-tin solder material is used both as the package interface layer and a protective seal ring, due to its capability to withstand high surface mounting temperatures (approximately 250 °C) and to provide good hermetic sealing. The concept is illustrated in Figure 1 below. This method of wafer level packaging is less complex and less expensive than existing

methods, as it provides hermetic encapsulations and electrical interconnections of the MEMS devices, as well as a solderable interface for surface mounting to the board. This method furthermore offers the ability to provide both die-level and device-level of packaging in a single step of wafer bonding and thus represents an attempt to significantly reduce packaging cost for RF MEMS.

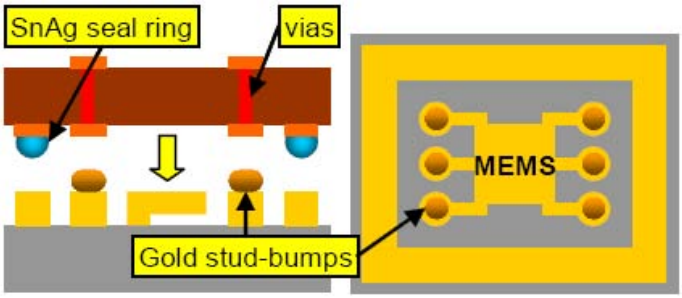


Figure 1. Illustration of a ceramic via wafer package [1].

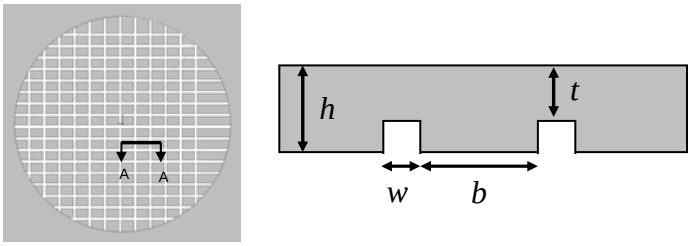
However, the difference in coefficient of thermal expansion (CTE) between the ceramic cap wafer and the silicon device wafer results in undesirable wafer curvature upon recovery from high temperature wafer bonding. Wafer curvature is concave on the side of the ceramic cap wafer because the coefficient of thermal expansion of ceramic is greater than that of the silicon wafer and the cap wafer shrinks more rapidly upon cooling to room temperature. There are two major problems with wafer curvature. From a practical handling standpoint, wafer curvature affects the later stages of dicing and device extraction. From a device reliability viewpoint, residual stresses induced in the gold-tin layer due to the thermal cooling may compromise hermetic sealing [2].

Analytical methods to relate curvature and stress include the well-known Stoney's equation for thin films as well as other methods such as a shape-energy method by Chen and Ou [3]. Suhir [4] also has developed an analytical model to determine thermally induced interface stresses and bow in circular substrate/film structure. However, due to the geometric complexity introduced by slotted wafers as well as non-linear thermal expansion, for the present work finite element simulation of wafer cooling is examined to predict wafer distortion. The simulations have been conducted using Abaqus form Dassault Systèmes (Providence, Rhode Island, USA).

Early investigation into this concept [2] suggested that the introduction of a slotted cap wafer has potential for reducing curvature. Understanding the effect of the slot parameters on the wafer curvature is necessary to choose optimal parameter values to minimize wafer curvature. Therefore, the primary objective of the present work is to conduct parametric design study of geometric modifications on ceramic cap wafers to reduce wafer curvature in thermo compression bonding through numerical simulations. A secondary objective is to enhance the simulation beyond earlier studies by including the temperature dependence of CTE for the ceramic cap wafers.

PARAMETRIC DESIGN STUDY

Finite element simulation of wafer cooling from 300 °C to 25 °C during wafer bonding process has been conducted to understand the effect of geometric discontinuities on wafer curvature. Parametric design study of wafer thickness, *h*, base width, *b*, bridge thickness, *t*, slot orientation, *c*, and slot width, *w*, results in 2^5 factorial design combinations. These geometric features are labeled in Figure 2. The response variable to minimize is wafer curvature, *k*, and Table I shows the factor levels of the design parameters. The values for the parameters were chosen based on practical considerations for wafer thickness, slot dicing, material availability, and device layout.



(a) (b)

Figure 2. Top-view layout of slotted LTCC cap wafer (a) and a partial cross-section (b) with labeled design parameters.

Table I. Slot design parameters with low (L) and high (H) values.

Design Parameters		
Wafer thickness *h*	L - 300 µm	H – 500 µm
Bridge thickness *t*	L - 50 µm	H – 250 µm
Slot orientation *c*	D- Down	U- Up
Base width *b*	L – 10 mm	H - 20 mm
Slot width *w*	1000 µm	5000 µm

FINITE ELEMENT SIMULATION

Material Properties

Relevant mechanical and thermal properties of silicon and LTCC are listed in Table II. The coefficients of thermal expansion of the wafers are initially assumed to be constant over the temperature for linear simulations, with values of 2.6 ppm/K (parts per million per degree Kelvin) for silicon and 5.5 ppm/K for LTCC.

Table II. Mechanical and thermal properties of Silicon and LTCC wafers [4].

Mechanical and Thermal properties of the wafers		
Properties	Ceramic Wafer	Silicon Wafer
Density (kg/mm3)	2.85E-06	2.40E-06
CTE (ppm/K) at room temperature	5.5	2.6
Young's modulus of elasticity (GN/mm2)	8.00E-05	1.60E-04
Thermal conductivity (W/mm·K)	3.00E-03	1.40E-01
Poisson's ratio	0.17	0.22
Specific heat (kJ/kg·K)	0.99	0.7

However, in refined examination (discussed subsequently below) CTE values are adjusted for nonlinear simulation according to the temperature dependence of CTE. Figure 3 and Figure 4 show the temperature dependent thermal expansion coefficient for the wafers and it is observed that for a temperature rise from 0 °C to 300 °C, the CTE of silicon and LTCC cap wafer increases by 32% and 38%, respectively.

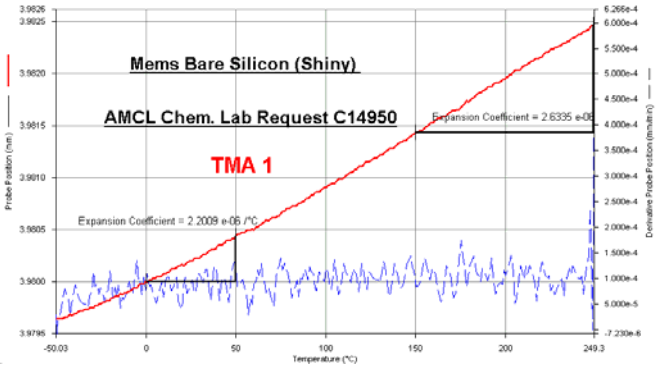


Figure 3. Temperature-dependent thermal expansion of bare silicon wafer.

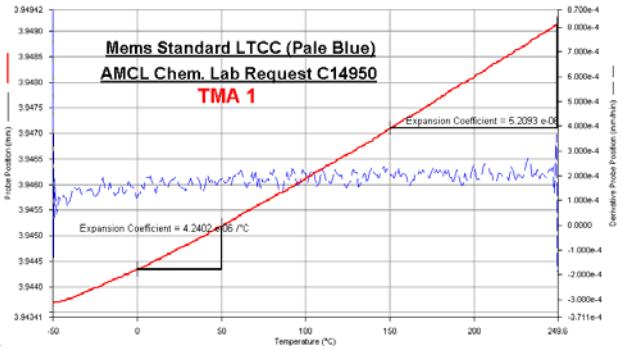


Figure 4. Temperature-dependent thermal expansion of LTCC.

Nonlinearity of CTE is more significant than the corresponding temperature dependence of Young's modulus of silicon and LTCC substrate. The temperature dependence of Young's modulus of silicon and alumina decreases by only 6% for the same temperature change [5, 6]. Hence, it is assumed that non-linearity of Young's modulus does not have strong effect on wafer curvature and Young's modulus of wafers is assumed to be constant for the finite element simulations.

MODEL FORMULATION

2-D Finite Element Model

Considering the periodicity and symmetric arrangement of slots, only two adjacent slots are considered to study the effect of slots on wafer curvature (see Figure 5). The thickness to diameter ratio of the wafers is very large and hence, 2-D plane strain formulation has been adapted for the numerical analysis.

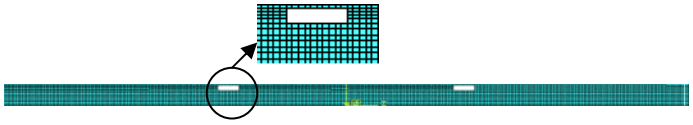


Figure 5. 2-D plane strain model of the bonded wafers.

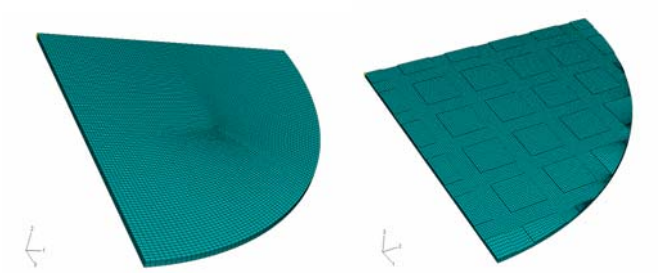
Mapped meshing with four-node linear heat transfer quadrilateral element (Abaqus type DC2D4) was chosen for heat transfer analysis problem. Four-node bilinear plane strain quadrilateral element (Abaqus type CPE4R) was chosen for the stress analysis. Symmetric boundary conditions were imposed on the model by constraining the left edge of the model in horizontal direction and constraining the node at the bottom left corner to restrict any movement. All other edges are kept free to permit bending during cooling.

The model results are consistent with the deformed shape when the wafers are subjected to cooling. The wafers assume concave shape as the CTE of LTCC cap wafer is larger than the CTE of silicon. The factorial design conditions were investigated by 2-D finite element analysis to examine the effect of slot parameters on wafer curvature and to achieve fast solutions. For this first study, all 32 design cases were assumed to have constant CTE and the design case that deflects least is considered the best case. Simulations are subsequently enhanced by incorporating nonlinear CTE for the baseline and the best cases.

3-D Finite Element Model

Benefiting from the symmetric arrangement of slots, only one quarter of the bonded wafers was considered for the analysis, as shown in Figure 6. A 3-D model of bonded wafers was meshed with eight node linear heat transfer brick heat transfer elements (DC3D8) for thermal analysis and 8 node

linear brick elements (C3D8R) for stress analysis. Symmetric boundary conditions were imposed on the straight edges of the model and the bottom node at the center was constrained in the thickness direction.



(a) Baseline case. (b) Slotted cap wafer case.

Figure 6. 3-D finite element model of bonded wafers.

The deformation in thickness direction for both linear and nonlinear coefficients of thermal expansion was examined for curvature comparison. The following are the assumptions made for the numerical study:

1. Silicon and ceramic materials are isotropic and linear thermo elastic.
2. Perfect bonding between coating and substrate exists.
3. Uniform temperature established in the body both at the processing temperature and at the temperature after cooling.
4. There are no mechanical compression forces acting on the wafers.

Analysis Details

Numerical simulation of wafer cooling from 300 °C to 25 °C was performed by first solving a pure heat transfer problem followed by stress/deformation analysis. Steady state thermal analysis of wafers was carried out to simulate thermal loading by setting the initial temperature as the bonding temperature 300 °C and the wafers are cooled to 25 °C. Nodal temperatures obtained from the analysis were stored as a function of time. The model is then copied to the stress model. Using the stored nodal temperature information as predefined data, stress and deformation analysis was conducted. The model correctly predicts concave curvature bending on the side of the ceramic cap wafer, and the maximum stress observed at the wafer interface agrees with physical reasoning.

RESULTS AND DISCUSSION

2-D Simulation Results

The deformation of the finite element model shows concave curvature toward the side of ceramic cap wafer, as the coefficient of thermal expansion of the ceramic under study is twice greater than the CTE value of silicon. Comparison of deflection between the design cases with slots and the baseline cases without slots reveals that the introduction of slots on the cap wafer reduces the wafer curvature. Examples of simulated results for deformation and stress of a typical slotted cap wafer case are shown in Figure 7.

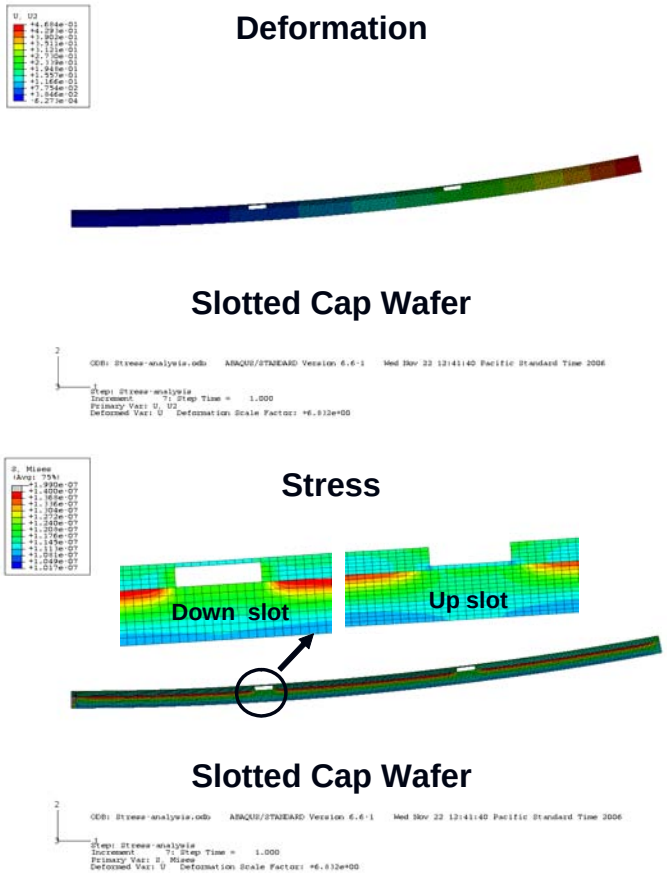


Figure 7. Examples of 2-D simulation results for predicting deformation and stress distribution for a slotted LTCC wafer bonded to a silicon device wafer.

As expected, thermal stress predicted through simulation is high at the interface between the ceramic cap wafer and silicon wafer material. In the case of cap wafers with slots, stress concentration is observed in the slot regions. The predicted wafer curvature for the baseline and the 2^5 factorial design cases are normalized by the curvature value of LTCC cap wafer without slot having 500 μm thickness (baseline case) and it is observed from Figure 8 that the lowest possible curvature is achieved by design case #21, for which slot parameters are 300 μm cap wafer thickness, 50 μm bridge thickness, 5 mm slot width, 10 mm base width. The deflection comparison of the baseline and the best cases reveals that wafer curvature can be reduced by 25% by introducing slots of above mentioned parameter combination on LTCC cap wafer.

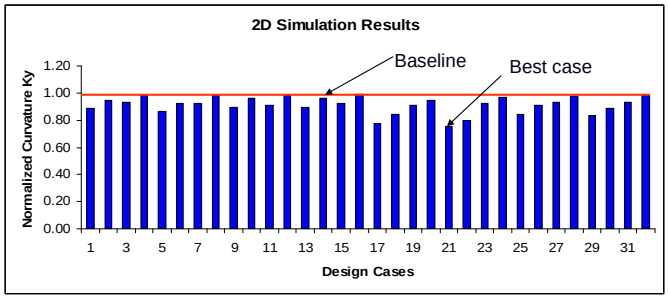


Figure 8. Graphical representation of the simulation results for all 2-D parametric design cases.

From Figure 8 it is noticed that all the design cases show reduction in curvature compared to default case as expected. It also shows that design cases with wafer thickness 300 μm show significant curvature reduction than design cases of 500 μm thick cap wafer, which implies that cap wafer thickness has strong effect on wafer curvature. The individual parameter effects on wafer curvature and the combination of the parameters are discussed in the next section.

The influence of nonlinearity of CTE on wafer curvature induced during thermal cooling was examined by incorporating temperature dependent CTE values for the baseline case and the best case. Linear simulation of wafer cooling assumes constant cap wafer CTE of 5.5 ppm/K. Nonlinear simulation incorporates temperature dependent CTE values in the finite element model. Therefore, the CTE difference between the wafers remains constant (2.9 ppm/K) in linear simulation and varies with temperature in nonlinear simulation. As CTE difference between the wafers during thermal cooling induces thermal stresses at the interface between the wafers, the change in CTE difference with respect to temperature in nonlinear simulation results in additional thermal stress and thereby increases wafer curvature.

By comparing the linear and nonlinear simulation results, it is evident that nonlinearity of CTE increases wafer curvature of baseline case by 7% and best case by 8%. It is also observed that the baseline case with 4.0 ppm/K for cap wafer predicts less curvature than the baseline case with 5.5 ppm/K and it is due to the fact that the former case has smaller CTE difference of 1.4 ppm/K than the latter case whose CTE difference is 2.5 ppm/K. As expected, the smaller the CTE difference, the lesser the wafer curvature.

Factor Effect Analysis

Five factor two level factorial 2-D design simulation results indicate that the introduction of slots in LTCC cap wafer reduces wafer curvature by 25%. However, the magnitude and direction of effect of individual factors and their combinations needs to be analyzed to better understand the significance of the slot parameters on wafer curvature. For 2^5 factorial simulations, estimation of factor main effects is made by finding the difference between the average radius of curvature at the high level of the factor and the average radius of curvature at the low level of the factor [7]. A high absolute value for an effect means that the factor responsible for it affects radius of wafer curvature significantly. A negative value means that increasing the level of that particular factor will decrease radius of wafer curvature. To reduce distortion, a large value for radius of curvature is desired.

It is evident in Figure 9 that bridge thickness has relatively large influence on wafer curvature followed by cap wafer thickness, and slot width. Both the bridge thickness and cap wafer thickness affects radius of wafer curvature in negative direction. Hence, an increase in cap wafer thickness and bridge thickness decreases radius of curvature. It is also observed that increasing the bridge thickness from 50 μm to 250 μm, the radius of curvature decreases by 94.4 mm and increasing the cap wafer thickness from 300 μm to 500 μm affects the radius of curvature by 66.7 mm. On the other hand, slot width affects curvature in the positive direction and an increase in slot width from 1 mm to 5 mm results in radius of curvature increase by 61.6 mm. The other two factor base width and slot orientation have slight influence on radius of curvature and the estimated effects are 37.9 mm and -7.77 mm, respectively and are relatively less significant when compared cap wafer thickness, bridge thickness, and slot width.

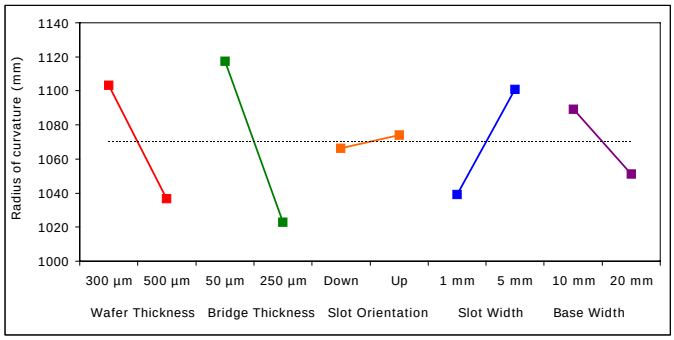


Figure 9. Graphical representation of the factor effects on wafer curvature.

3-D Simulation Results

3-D finite element simulation results suggests that wafer curvature decreases by 34% by introducing slots in cap wafer and incorporation of nonlinearity of CTE in the model increases the wafer curvature by 7.4%. High interfacial stresses developed at the interface between the silicon and LTCC wafers are captured in the stress plot of baseline case, whereas thermal stresses are distributed evenly at the bottom surface of the slots and stress concentration areas are observed at bottom slot corners.

2-D vs. 3-D Simulation Results

For the baseline case, both 2-D and 3-D simulation results vary by only 2%. For the slotted cap wafer case, 2-D predicted curvature value is more than 3-D prediction and the variation is 20%. The higher curvature value of 2-D simulation can be explained from Figure 10 that 2-D simulation considers only the effect of lateral slots whereas 3-D simulations consider slots in both the lateral and longitudinal directions. A graphical comparison of linear and nonlinear simulations for both 2-D and 3-D models is shown in Figure 11.

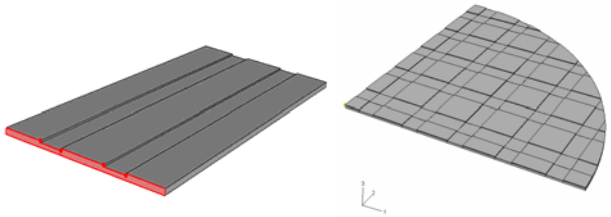


Figure 10. (a) 2-D plane strain and (b) 3-D finite element models.

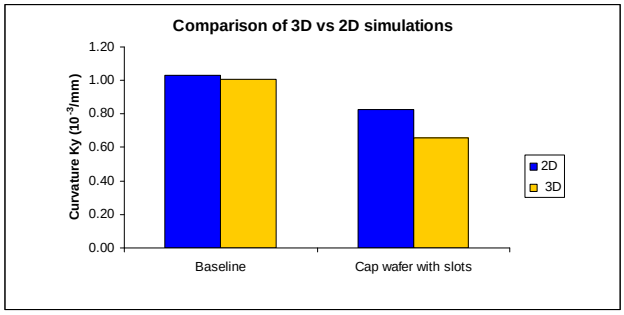


Figure 11. Comparison of 3-D vs. 2-D simulation. Without slots there is not much difference in predicted curvature, but the difference between 3-D and 2-D simulation is more pronounced for slotted wafers.

Simulation vs. Experimental Results

Predicted results have been compared with radius of wafer curvature from previous work [8] measured from coordinate measuring machine (CMM). The actual deformation in bonded wafers is consistently lower than predictions. For example, the maximum deflection for a 500 µm cap wafer with CTE value of 4.0 ppm/K is predicted by 3-D model to be 1280 µm, but measured to be only 1030 µm. The discrepancy is greater for wafers with CTE of 3.4 ppm/K, where the FEA model predict 670 µm but actual wafers were measured to have only 220 µm maximum deflection. Imperfect model assumptions include full surface-to-surface bonding between wafers and absence of any mechanical clamping during bonding. There may also be differences in material properties other than CTE (e.g. Young's modulus, Poisson's ratio) compared to standard values assumed in the numerical model. Furthermore, it should be noted that the wafer-to-wafer measurement variability is about 40 µm even for identical wafers [8].

CONCLUSIONS AND FUTURE WORK

Parametric design study of 2^5 factorial 2-D design simulations of wafer cooling from 300 °C to 25 °C were carried out in Abaqus to examine the effect of slot parameters on wafer curvature and the study was aimed at reducing the wafer curvature due to thermal mismatch by optimizing the slot parameters. 3-D simulations on the baseline and the best case that yields the lowest possible wafer curvature were compared with 2-D simulations. Finally, 3-D simulation results were compared with experimental CMM measurements of radius of curvature. From the simulation results and factor effect analysis, it is observed that:

1. The introduction of slotted cap wafers in LTCC cap wafers has potential to reduce wafer curvature by 25% or more.
2. Of the slot parameters, within their respective practical limits depth, width and spacing are all influential at comparable magnitudes. Wafer thickness is also important, but slot orientation is not.
3. Including temperature-dependence of CTE in the simulation model increases predicted curvature by 7-8%.
4. 2-D vs. 3-D comparison shows that 2-D plane strain over-estimates curvature and the difference is more pronounced with slotted wafers.
5. Wafer-to-wafer variability is very appreciable, and obscures the quantitative benefit of using slotted wafers.
6. Numerical vs. experimental comparison shows that FEA simulation overestimates curvature.

The discrepancy between FEA model and experimental results is attributed to multiple factors. The primary areas for improvement and future work in the model are to represent explicitly the gold interlayer, and to account for a two-stage deformation with mechanical clamping at high temperature followed by distortion under the resulting pre-stress. As was done with experimentally determined CTE values, the model can also be made more exact by using pre-characterized mechanical properties rather than values from standard reference tables.

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