crease in cell impedance. The cycle life of laboratory cells is virtually always Li-limited. On the other hand, the cycle life of the 5 Ah cells seems to be electrolyte limited, and especially so when the electrolyte is the lower conducting 2Me-THF/$LiAsF_6$ (1.5*M*). Our analytical data to date indicate that the electrolyte salt is slowly consumed with cycling (4). As this happens, the internal impedance increases, lowering the rate capability of the cell. Eventually, the cell develops dendrite shorts and it fails. When the electrolyte is the lower conducting 2Me-THF/$LiAsF_6$, the cell experiences larger resistance polarizations, with the result that the constant current discharge capacity falls off more rapidly with cycling. This may be the reason why the capacity *vs.* cycle-life profile in Fig. 9 takes on two separate routes with the two solutions.

Conclusions

While a high solution conductivity and a high concentration of $LiAsF_6$ are desired for high rate discharge compatibility of Li/TiS_2 cells at room temperature, these properties have had little predictive value with respect to the cell's low temperature (*e.g.*, −20°C) performance. At low temperatures, THF:2Me-THF/$LiAsF_6$ mixed solutions, despite their lower conductivity, have allowed better discharge performance than have THF/$LiAsF_6$. The superior low temperature performance of the mixed ether solutions is believed to be related to the structure and properties of the Li^+-$(ether)_n$ solvates that exist in such solutions. ^{13}C NMR measurements revealed that in the mixed solutions, both THF and 2Me-THF complex Li^+ to the same extent as each does in its individual solutions, suggesting the existence of structurally disordered Li^+-solvates in the mixed media. Such solvates seem to favor better low temperature Li^+ transport, perhaps reflective of a more desirable environment for better Li^+ diffusivity. In $LiAsF_6$ solutions in THF or 2Me-THF, structurally more ordered complexes apparently exist, rendering a higher degree of stability to the Li^+-solvates and a related lower Li^+ diffusion. A high Li cycling efficiency in THF/2Me-THF mixed solutions has been achieved by the use of 2Me-F as an additive. A fruitful approach to improving the low temperature performance of liquid electrolyte Li batteries seems to be the search for mixed solutions that form structurally highly disordered Li -solvates.

Acknowledgment

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Low Temperature Surface Cleaning of Silicon and Its Application to Silicon MBE

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ABSTRACT

A low temperature thermal cleaning method for Si molecular beam epitaxy (MBE) is proposed. This method consists of wet chemical treatment to eliminate carbon contaminants on Si substrates, thin oxide film formation to protect the clean Si surface from contamination during processing before MBE growth, and desorption of the thin oxide film under UHV. The passivative oxide can be removed at temperatures below 800°C. It is confirmed that Si epitaxial growth can take place on substrates cleaned by this method and that high quality Si layers with dislocations of fewer than 100/cm^2 and high mobility comparable to good bulk materials are formed. Surface cleanliness, the nature of thin passivative oxide films, and cleaning processes are also studied by using such surface analytic methods as Auger electron spectroscopy, reflection high energy electron diffraction, and x-ray photoelectron spectroscopy.

Si molecular beam epitaxy (Si-MBE) has been shown to produce device quality epitaxial Si films. This can, however, be obtained only when a clean silicon substrate surface is prepared before epitaxial growth. That is, contaminants on the substrate, such as oxide and carbide, prevent layer growth and become the main causes of crystal defects in the epitaxial layers. In order to provide clean surfaces and eliminate defect origins at interfaces, high temperature thermal etching at about 1200°C prior to epitaxial growth has been commonly used in an ultra-high vacuum (UHV) (1-5). However, this technique causes undesirable impurity diffusion and changes the designed impurity concentration profile within the Si substrate. Furthermore, crystal defects, such as dislocations and stacking faults, tend to increase and slip lines are often generated across the Si substrate during high temperature treatment. Thus, it is important to find a low temperature surface cleaning method in which the temperature can be lowered to below 900°C.

Several studies have reported low temperature surface cleaning techniques. The methods used include ion sputtering (6, 7), laser annealing (8, 9), "galliation," in which the substrate is exposed to a gallium vapor beam at about 800°C substrate temperature in UHV (10), and exposure to a Si beam (11). Ion sputtering, however, produces undesirable radiation damage at the surface and point defects often remain even after annealing. Galliation is effective in removing silicon oxide, but complete removal of Ga atoms from the Si surface and no Ga diffusion into the Si substrate have not yet been fully confirmed. Also, for the

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Si beam cleaning method, complete removal of carbon contaminants has not been certified.

In order to overcome the drawbacks of these low temperature surface cleaning methods, a new surface cleaning method was proposed by the authors and preliminary results were reported (12). In this paper, the details of this method are described, and characterization of the cleaned Si substrates and the epitaxial films grown on the cleaned substrates is also reported. This low temperature cleaning method consists of two processes. Wet chemical treatment is the first process and is done for etching the contaminated surface layers and for formation of a contamination-free passivative oxide film on the Si substrate. The second process is heating under UHV at temperatures below 900°C to remove the oxide film through thermal etching and obtain an atomically clean surface.

To evaluate this cleaning method, MBE growth was also carried out on Si wafers prepared in various ways, and it was revealed that good quality epitaxial films can be obtained on Si substrates treated by the technique developed here.

This surface cleaning method is thought to also be very useful for basic studies of Si surfaces. This is because the thermal stress and formation of thermal etch pits during the cleaning process are much less than that for the high temperature method which has been commonly used in the field of surface physics and chemistry.

Guidelines for low temperature surface cleaning of a Si surface, which were obtained through analysis of conventional high temperature thermal etching processes, are described here before proceeding to the experimental results. The Auger spectra of Si surfaces, treated by the high temperature method, are shown, in Fig. 1, as a function of the substrate temperature. After conventional wet chemical treatment, O_{KLL} (515 eV) and C_{KLL} (272 eV) Auger signals, which originate from surface contaminants, were observed. When the sample was heated to 850°C, the O_{KLL} and oxidized Si_{LMM} (75 eV) peaks disappeared, but the C_{KLL} peak remained. The fact that the oxide film on Si is removed at temperatures between 800° and 1000°C in a vacuum was first reported by Lander and Morrison (13). The removal of carbon is more difficult than oxide, and the C_{KLL} peak disappears only after heating above 1100°C. This is the reason why the high temperature (above 1100°C) treatment is necessary to obtain clean Si surfaces. Therefore, if a carbon-free oxidized Si surface can be prepared, low temperature thermal etching for surface cleaning is possible.

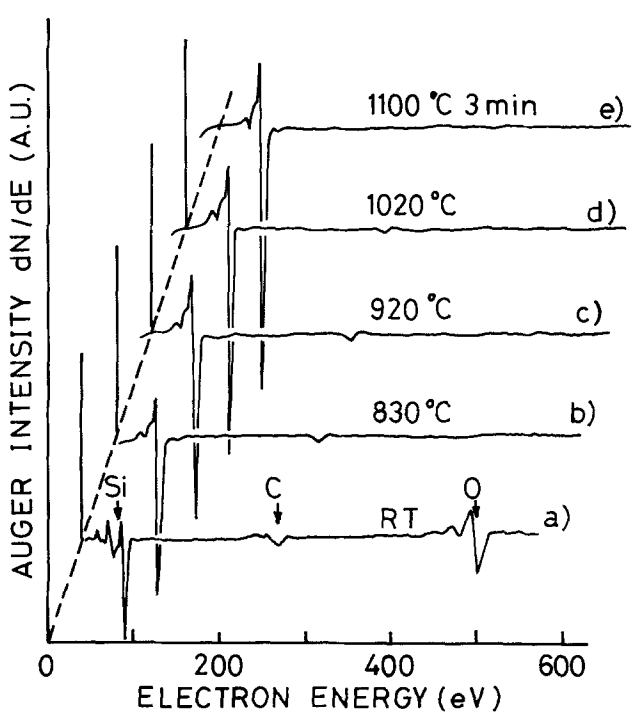

Fig. 1. *In situ* Auger spectra of Si surfaces cleaned by the conventional high temperature thermal etching method. (a) As-freshly oxidized, (b) after heating at 830°C, (c) 920°C, (d) 1020°C, and (e) 1100°C.

The following is our basic idea for obtaining clean Si surfaces at low temperatures. (*i*) Oxide film is grown by chemical treatment on the Si substrate as a passivation film. Since the oxide surface is much less active than the bare Si surface, there are fewer carbon contaminants on the oxidized Si surface, and they can be removed more easily than those on the Si surface. (*ii*) Active sites on the oxide surface, where contaminants are easily adsorbed, are decreased by forming a smooth surface through repetition of the chemical oxidation and etching processes. (*iii*) Active sites which still remain on the oxide surface are decorated with unstable adsorbants, such as Cl atoms, before the carbon atoms are adsorbed. These adsorbants can be removed more easily by heating than can the oxide film. (*iv*) The oxide film is removed by heating under UHV. It must, therefore, be very thin and volatile. If these conditions are satisfied, an atomically clean Si surface can be obtained at relatively low temperatures.

Experiment

The Si single crystal substrates used in this work were 50 mm diameter mechanochemically mirror polished wafers. Various types of substrates, *i.e.*, n-type (P doped), p-type (B doped), and (100) and (111) oriented, were used.

The Si substrates were initially prepared by wet chemical processes. The chemical treatment consisted of three steps. The first step was a degreasing process, the second was elimination of the contaminants on the Si substrate, and the third was formation of a passivative oxide film on the Si substrate. Details of these treatments are described in Table I. It should be pointed out that several repetitions of boiling in an HNO_3 bath and removal of the oxide layers completely eliminate carbon contaminants on the substrate. As a final chemical treatment, a very thin oxide film was grown in a solution of $HCl:H_2O_2:H_2O$

Table I. Cleaning specifications

1. Degreasing

Rinse in overflowing deionized water for 10 min.
Rinse twice in methyl alcohol bath for 5 min with agitation.
Boil in trichlorethylene bath for 15 min.
Rinse twice in methyl alcohol bath for 5 min with agitation.
Rinse in overflowing deionized water for 10 min.

2. HNO_3 boiling

Boil in HNO_3 bath at 130°C for 10 min to etch Si surface region and to form the oxide layer.
Dip in 2.5% HF solution for 10-15s, to remove the oxide.
Rinse in overflowing deionized water.
Check the surface. If the surface does not dry uniformly, the HNO_3 boiling procedure is done once again. Generally, 3-4 repetitions are performed.

3. NH_4OH boiling (alkali treatment)

Boil in a solution of $NH_4OH:H_2O_2:H_2O$ (1:1:3) at 90°C for 10 min to make a thin surface oxide.
(Mix NH_4OH and H_2O and bring to temperature. Just prior to use, add H_2O_2.)
Dip in 2.5% HF solution for 10-15s, to remove the oxide layer.
Rinse in overflowing deionized water.

4. HCl boiling (acid treatment)

Boil in a solution of $HCl:H_2O_2:H_2O$ (3:1:1) at 90°C for 10 min to make a thin surface oxide.
(Mix HCl and H_2O and bring to temperature. Just prior to use, add H_2O_2.)
Rinse in overflowing deionized water for 10 min.
Check that the surface uniformly becomes wet.
Spin dry.

Chemicals used in this work were not specifically purified but commercial reagents were guaranteed as:
HNO_3: 64-66 w/o assay with less than 2 ppm impurities;
HCl: 35-37 w/o assay with less than 7 ppm impurities;
H_2O_2: 30 w/o assay with less than 40 ppm impurities;
NH_4OH: 28-30 w/o assay with less than 10 ppm impurities;
HF (50%), methyl alcohol and trichlorethylene: semiconductor grade, deionized water: 14-15 MΩcm.

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at 90°C for 10 min to protect the substrate from chemisorption of such contaminants as carbon.

After chemical treatment, the sample was mounted very loosely between densified high purity graphite rings situated on the Ta heater assembly. Any direct contact between the sample and the metal components was avoided to prevent reaction between the Si and the metals. A loose holding prevents generation of slip lines from the contacts. The sample holder was then loaded into a commercial MBE instrument (Vacuum Generators, Model 366) consisting of a three-chamber system composed of a first entry lock, an analysis chamber, and a growth chamber. The base pressure of the growth chamber was lowered to about 2×10^{-11} torr by using diffusion pumps, Ti sublimation pumps, and liquid nitrogen cryo-panels.

The samples were heated at temperatures varying between 680°-930°C for periods of 5-60 min in UHV to obtain clean surfaces. Sample temperature in UHV was measured by a pyrometer in which only light with a wavelength around 0.7 μm could be detected. Since the Si substrate is opaque at this wavelength, the real substrate temperature could be determined, even though the back side of the Si wafer directly faced the Ta heater. The emissivity of the Si at this wavelength was calibrated in advance using a conventional furnace.

Surfaces were characterized *in situ* using Auger electron spectroscopy (AES) and reflection high energy electron diffraction (RHEED) methods.

After surface characterization, Si epitaxial films were grown on the Si substrates. An Si molecular beam was produced by an electrostatically focused electron bombardment source. For n-type doping, an Sb molecular beam was produced by a conventional effusion cell with a p-BN crucible. Growth rate, substrate temperature, vacuum pressure during growth, and thickness of grown layers were about 1 Å/s, 650°-800°C, about 10^{-9} torr, and 1 μm, respectively.

Carrier concentration and mobility of the Si epitaxial layers were determined by Hall measurements, where a six-electrode bridge pattern was formed by conventional photolithography and metha-etching processes. Dislocation density in Si epitaxial layers was estimated by Secco's etching method.

Results and Discussion

Surface cleaning by low temperature thermal etching method.—Figure 2 shows the Auger spectra as a function of the heating temperature in UHV. The spectrum (a) was measured immediately after loading a (111) wafer into the MBE chamber. It can be seen that a very thin oxide layer is formed on the Si substrate after the chemical treatment. No discernible traces of the C_{KLL} peak are observed. This result is in striking contrast to previously reported results (5). That is, carbon contaminants always remained on the Si oxide in the previous reports. The small peak at 182 eV is due to the LMM transition of Cl atoms caused by ($HCl + H_2O_2 + H_2O$) boiling treatment. This peak, however, is not observed after heating at 550°C for sample degassing, as shown in Fig. 2(b). It was later confirmed that this peak disappears at around 400°C. During the degassing process, the relative intensity of the peak at 92 eV, assigned to elemental Si_{LMM} transition, to the peak at 75 eV, due to oxidized Si, and to the O_{KLL} peak exhibited no change. This shows that the oxide film on the Si was not removed during the degassing process. An Auger spectrum of the sample after heating at 785°C for 15 min is shown in Fig. 2(c). The peaks from the oxide film, that is the Si_{LMM} (75 eV) and O_{KLL} peaks, disappear, and only the contamination-free elemental Si_{LMM} (92 eV) peak can be observed.

A RHEED pattern for Si wafers treated in this way is shown in Fig. 3. A clear (111)-7 × 7 superstructure is seen (Fig. 3(a)), and superposition of the RHEED pattern due to silicon carbide, which is frequently observed when Si is heated in vacuum, was not observed at all. It can, therefore, be said that an atomically clean surface is obtained by the new low temperature thermal etching method.

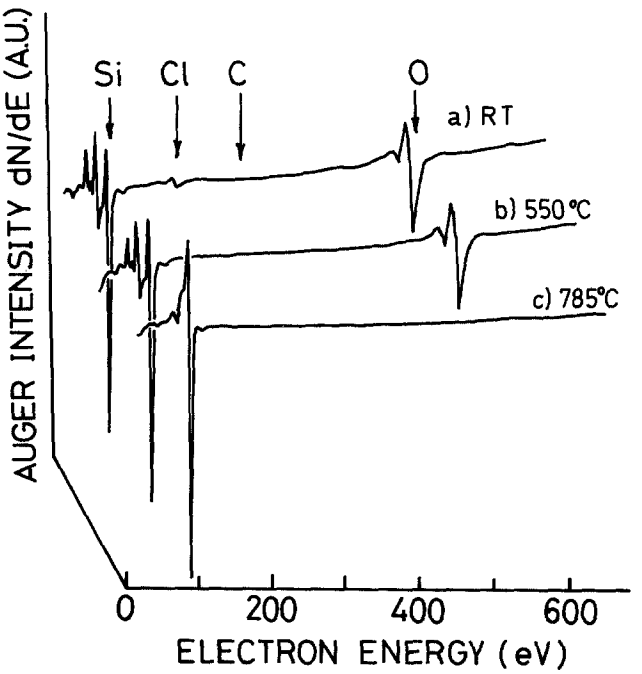

Fig. 2. *In situ* Auger spectra of Si surfaces cleaned by the low temperature thermal etching method. (a) As-freshly oxidized, (b) after heating at 550°C for 15 min, (c) after heating at 785°C for 15 min.

As mentioned before, in order to easily desorb the passivation oxide layer, the thinner the oxide, the better. So, the thickness of the oxide is one of the important subjects. Uncertainty, however, exists in estimating the thickness from AES intensity data, since electron escape

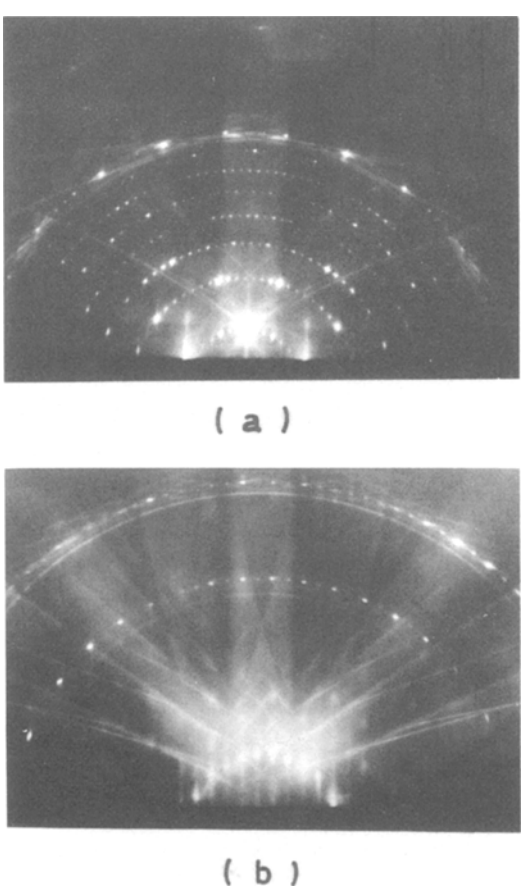

Fig. 3. RHEED patterns of Si surfaces after thermal cleaning at 785°C for 15 min. (a) For (111) substrate, where the incident beam direction is parallel to [112]. The 7 × 7 superstructure is observed. (b) For (100) substrate, where the incident beam direction is parallel to [110]. The 2 × 1 superstructure is observed.

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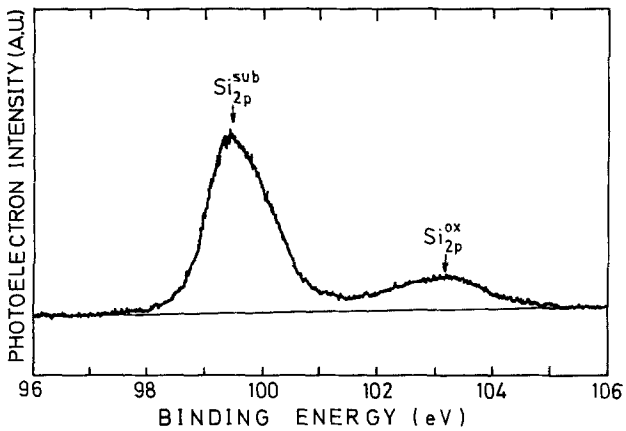

Fig. 4. Si_{2p} photoelectron spectrum of Si surface after (HCl + H_2O_2 + H_2O) boil treatment. $Mg_{K\alpha}$ was used. Photoelectron acceptance angle of the analyzer was 42°.

depth and Auger transition probability change for different materials such as SiO_2 and Si. The oxide thickness formed by the new chemical treatment was, therefore, determined by x-ray photoelectron spectroscopy (XPS), since the relationship between photoelectron intensity and thickness for very thin thermally oxidized silicon has already been clarified (14). The Si_{2p} photoelectron spectrum of a Si wafer after chemical treatment is shown in Fig. 4. The peak at 99.4 eV binding energy corresponds to the Si substrate, and that at 103.2 eV corresponds to the oxide film. Since the chemical shift measured for the oxide film is 3.8 eV, the oxide film is thought to be SiO_2. Thickness of the oxide film can be determined from the peak intensity ratio of the oxide peak to the substrate peak. The peak intensity ratio obtained is about 0.22, and the estimated oxide thickness is approximately 6.4Å, using Eq. [14] in Ref. (14). The thickness of the oxide formed by the method developed here was found to vary from 5 to 8Å, from sample to sample.

Temperature for removing this thin oxide film could be lowered to 710°C, which is the lowest recorded temperature that has produced a contamination-free clean Si surface by thermal etching. Figure 5 shows Auger spectra as a parameter of heating time at 710°C.

Lander and Morrison showed (13) that the very thin oxide film on Si is removed, as vaporized SiO, according to a reaction of

$$Si + SiO_2 \rightarrow SiO \uparrow$$

This removal process seems to be conducted in two steps,

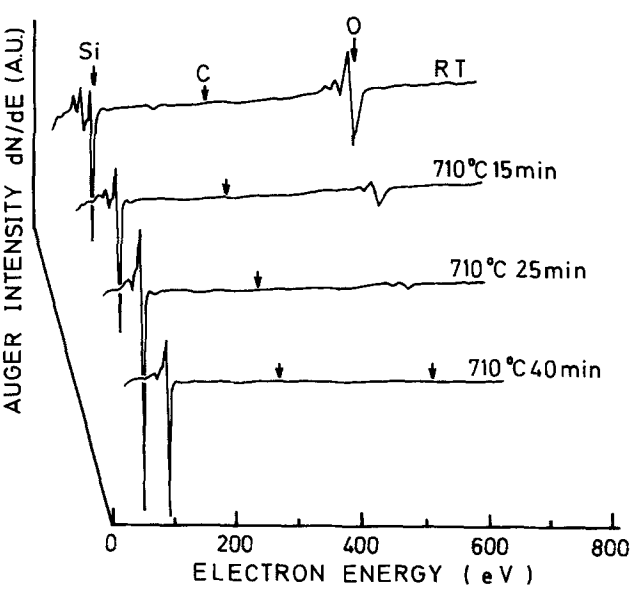

Fig. 5. *In situ* Auger spectra of Si surfaces after iso-thermal heating at 710°C.

the reaction between Si and SiO_2 at the interface, and the migration of atoms through the oxide film. To evaluate which process dominates the thermal etching process, the oxide thickness was measured as a function of heating time. The oxide thickness was estimated from AES and XPS data.

The relation of oxide thickness (d) and AES intensity ratio $I_{O_{KLL}}$ (515 eV)/$I_{Si_{LMM}}$ (92 eV) is presented as Eq. [1]

$$I_{O_{KLL}}(515\text{ eV})/I_{Si_{LMM}}(92\text{ eV}) = C \cdot \{1 - \exp(-d/\lambda_{O_{KLL}} \cdot \cos\theta)\}/\exp(-d/\lambda_{Si_{LMM}} \cdot \cos\theta) \quad [1]$$

where θ is 42 degrees for the cylindrical mirror analyzer used here, λ is electron escape depth, C is a constant and expressed as

$$C = K \cdot \gamma_{O_{KLL}} \cdot n_O \cdot \lambda_{O_{KLL}}/(\gamma_{Si_{LMM}} \cdot n_{Si} \cdot \lambda_{Si_{LMM}})$$

where K is analyzer instrument constant, γ is Auger transition probability, n is number of atoms in the material. Johannessen *et al.* reported values of $\lambda_{O_{KLL}}$ and $\lambda_{Si_{LMM}}$ as 13Å and 5Å, respectively (15). Since the thickness obtained by the XPS method is 6.4Å, as mentioned before, and Auger intensity ratio $I_{O_{KLL}}$ (515 eV)/$I_{Si_{LMM}}$ (92 eV) is 0.38, C is determined to be 0.14. Once the constant C is determined, the oxide thickness can be estimated only from the AES data using Eq. [1]. Figure 6 shows the oxide thickness obtained in this way as a function of heating time at 710°C. As seen in this figure, the decrease in the oxide thickness bears a linear relation to heating time. This result indicates that the process dominating thermal etching is not the migration of atoms through the oxide film but the reaction at the Si-oxide interface. This might be due to the fact that the oxide film is very thin.

For (100) wafers, the same kind of cleaning results were obtained, and a (100)-2 × 1 superstructure was observed by RHEED measurement as shown in Fig. 3(b). Only a pure Si Auger peak was observed after cleaning. However, the lowest temperature that obtained a clean (100) surface was found to be a little higher than that for (111) surfaces, *i.e.*, about 750°C. This temperature difference might come from the fact that the bonding energy for a (100) surface is higher than that for a (111) surface, since the number of the surface bonds of the uppermost Si atom on a (100) surface is two, while that for a (111) surface is one.

It may be important to make some additional remarks on a chemical treatment as a final step of the process.

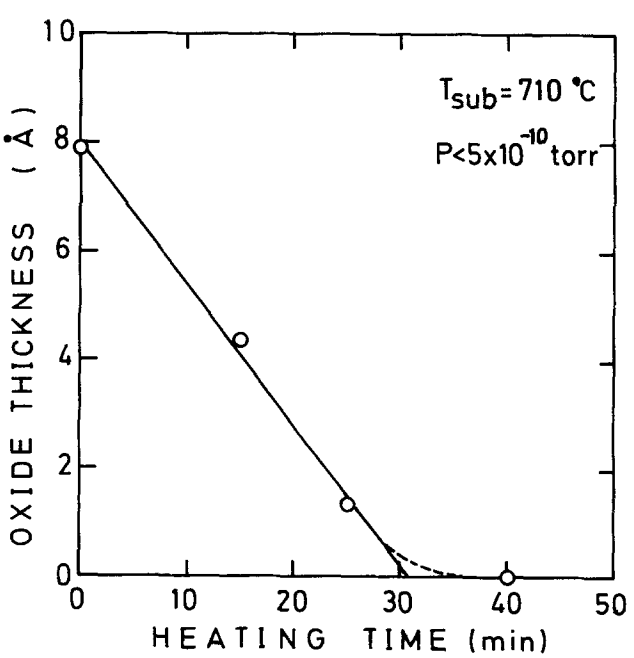

Fig. 6. Relationship between the oxide thickness on Si substrate and heating time at 710°C.

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HNO_3 boiling treatment instead of ($HCl + H_2O_2 + H_2O$) treatment is also suitable as a final oxide formation chemical treatment, if the carbon contaminants on a Si wafer are completely removed by repetition of formation and removal of the oxide film by HNO_3 boiling and HF dipping. Furthermore, ($NH_4OH + H_2O_2 + H_2O$) boiling is also effective as a final chemical treatment, although the oxide removing temperature is different among the treatments, *i.e.*, 850°C, 780°C, and 715°C for HNO_3 boiling, ($NH_4OH + H_2O_2 + H_2O$) boiling, and ($HCl + H_2O_2 + H_2O$) boiling, respectively. Comparing these chemical treatments, the existence of O_2 gas and/or atomically activated oxygen in the solution from the addition of H_2O_2 seems to be helpful in growing a volatile thin oxide film on a Si substrate. Recently, new chemical treatments, *i.e.*, an ozone gas reaction method under ultraviolet light (16), where the removal of contaminants and formation of oxide are carried out, has been proposed. Although surface characterization after these treatments has not been fully performed, these methods are very interesting as prior treatments for Si-MBE, and low dislocation density of Si-MBE films have been reported. The most important conclusion about chemical treatment is that, although there are various successful chemical treatment methods, the essence is to obtain the very thin volatile passivative oxide films with contamination-free surfaces on Si substrates.

Application to Si-MBE.—Silicon epitaxial growth was performed on a Si substrate treated by the method developed here. The epitaxial films grown here showed very sharp and clear RHEED spots and Kikuchi lines, and 7 × 7 and 2 × 1 superstructures were observed for the (111) and (100) substrates, respectively, indicating good crystallinity in the grown Si layers.

The surface morphology of the epitaxial films on (100) and (111) substrates was very smooth and mirror-like. As pointed out by Henderson (5) and also Konig *et al.* (17), the epitaxial growth of Si films can take place even on carbon contaminated substrates if the amount of carbon is not excessive. These epitaxial films frequently appear defect free at first sight. Specifically, surface observation using a differential interference microscope, x-ray topography, or electron diffraction experiments shows smooth, defect-free epitaxial layers. However, more precise experiments have revealed that when the usual peroxide cleaning method is employed, dislocation density decreases as thermal etching temperature increases, and a temperature of 1200°C is required for the dislocation density to be reduced to below 1000/cm^2. Moreover, etching evaluations of crystal defects have revealed that epitaxial films grown on such substrates possess many point defects, even though the film gives clear diffraction spots and Kikuchi lines in electron diffraction. It is obvious that such defects reduce the performance of various types of devices. Therefore, complete elimination of carbon contaminants is important for growing high quality epitaxial films.

Figure 7(a) shows a differential interference microphotograph of Secco's etched nondoped Si-MBE film on (100) substrate with the new cleaning method employed. Ota has reported the chemical etching method for evaluating the variety of defects in Si-MBE films in detail (18). The density of the dislocation etch pits that appear circular or elliptical, similar to Ota's results, is less than 100/cm^2. This defect density is considered very low for an MBE film. To reduce the defect density, the MBE instrument must be installed in a clean room.

Figures 7(b) and (c) show the surface morphology after Secco's etching for Sb-doped Si-MBE films on (100) substrates. The microscopic surface roughness of the doped samples increased as the dopant concentration increased. This shows that the point defects and/or clustered crystallographic imperfections increase as the dopant concentration increases. This tendency is commonly observed in doped samples and it is not thought to be strongly dependent on the surface cleaning method.

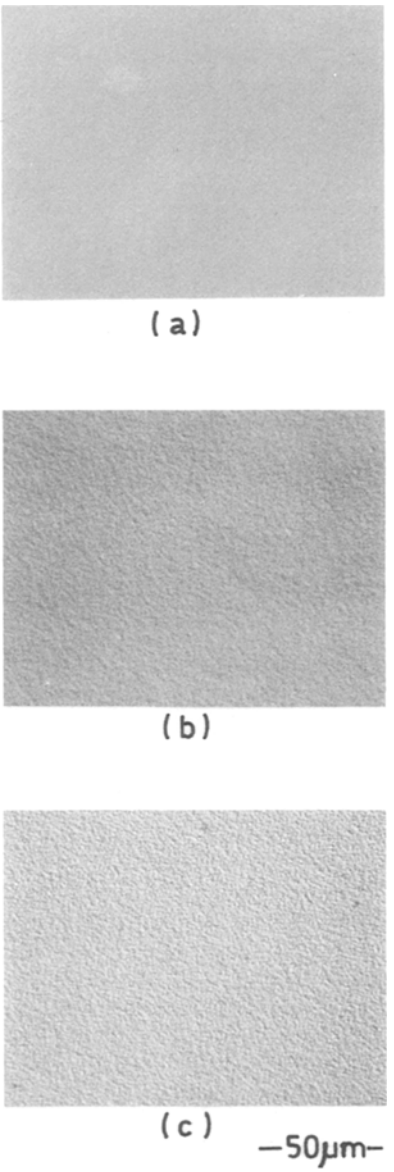

Fig. 7. Optical differential interference microphotographs of Secco's etched Si-MBE layers grown on (100) substrates. (a) Undoped Si-MBE film, (b) 2 × 10^{17}/cm^3 Sb doped Si-MBE film, and (c) 4 × 10^{18}/cm^3 Sb doped Si-MBE film.

To characterize the electrical properties of the Si epitaxial layer, a Hall measurement was carried out. Figure 8 shows the electron drift mobility as a function of impurity concentration for Sb-doped Si-MBE films. The solid curve presents the Irvin relation for bulk Si crystal (19, 20). The data for Si-MBE films closely match the

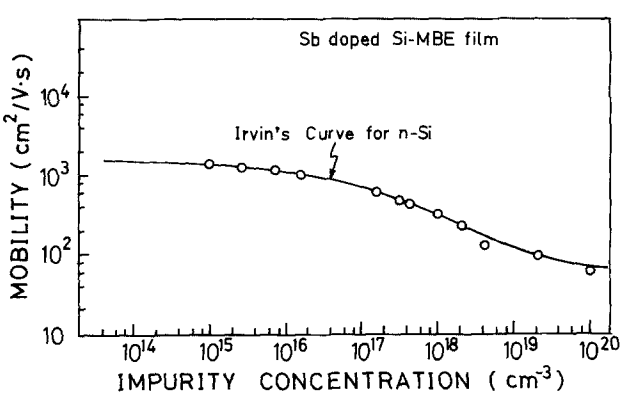

Fig. 8 Electron drift mobility of Si-MBE films as a function of Sb concentration.

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Irvin curve in the wide range of impurity concentration from 1×10^{15} to $1 \times 10^{20}/cm^3$. That is, the Si-MBE film has high mobility, comparable to that of bulk crystal. It is noted that this high carrier concentration, in the range of 10^{20} cm^{-3}, exceeds the doping limitation in the case of neutral beam dopants. This is due to the use of an electrostatic electron gun as the Si molecular beam source. Details on doping efficiencies concerning Si evaporators and dopants will be reported elsewhere.

The results obtained here show that this new cleaning method for Si substrates is effective for Si-MBE technology. The standard round silicon wafers used in this experiment are compatible with conventional silicon processes, and the cleaning technique can easily be applied to larger round wafers with diameters greater than 100 mm. Therefore, it may be concluded that this low temperature thermal cleaning technique has eliminated a large obstacle to the application of Si-MBE in practical processes and has thus increased Si-MBE feasibility.

Conclusion

The purpose of this study was to develop and characterize the surface cleaning method as a pretreatment for Si substrates to be used for Si-MBE. The results are as follows: (*i*) Careful chemical treatment can protect a Si substrate surface with a thin passivative oxide layer from carbon contamination. Thickness of this oxide layer is estimated to be 5-8Å. Atomically clean silicon surfaces can be obtained at temperatures lower than 800°C by thermal desorption of the oxide layer in UHV. The desorption process of oxide film on Si seems to be dominated by the reaction between Si and SiO_2 at the interface. (*ii*) Highly crystalline silicon epitaxial films can be grown on Si substrates treated by the surface cleaning method. The dislocation density in the epitaxial film is less than $100/cm^2$. The carrier mobility of the Si-MBE film is acceptable and comparable to that of bulk crystal throughout the wide range of doping concentration from 1×10^{15} to $1 \times 10^{20}/cm^3$.

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Potentiodynamic and Galvanostatic Stripping Methods for Characterization of Alloy Electrodeposition Process and Product

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ABSTRACT

Potentiodynamic and galvanostatic stripping techniques have been applied towards the characterization of zinc-nickel alloy deposition process and product. The current-potential relations required to recover the equilibrium and kinetic properties of alloys have been obtained for the eutectic, solid solution, and intermediate phase types of alloys. The galvanostatic stripping response shows a series of plateau regions, and the potentiodynamic response reveals a peak structure. These stripping responses have been employed to determine the chemical and phase compositions of electrodeposited zinc-nickel alloys, evaluate their corrosion resistance, and estimate the equilibrium potentials of various zinc-nickel phases (α, γ, and η-phases). The zinc-nickel deposition process has been characterized through evaluation of partial currents due to alloy components and the current efficiency of alloy deposition. The design of multiple layered zinc-nickel alloy films for the protection of steel is discussed on the basis of the accelerated corrosion behavior of the γ-phase and the equilibrium potentials of the phases.

There is considerable interest in the electrodeposition of alloy coatings for corrosion protection (1, 2) and electrocatalysis (3, 4), and also for their electrical, mechanical, and magnetic properties (5, 6). Some of the unique features of electrodeposited alloy coatings are their metastable nature (supersaturated phases and mixtures of phases), fine grain structure, altered defect structure with peculiar dislocations and packing defects (5), and nonmetallic inclusions such as O, H, S, P, C, etc., in the deposited material (6). Each of these features can be controlled by a proper choice of deposition conditions and can hence be used to produce materials with the desired properties. In view of the complexities associated with electrodeposited alloys, *in situ* techniques are re-

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