Inductively Coupled Plasma Etching of SOI and its Applications in Submicron Optical Waveguide Devices

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ABSTRACT

SOI promises a good platform for dense integration of optical devices. However, as dimensions scale down, propagation losses mainly caused by the scattering loss at sidewall had been serious problems. ICP etching of SOI is proved to be an available anisotropic etch technique to make submicron optical waveguide devices. With the help of e-beam lithography, We fabricated Single-mode submicron rib SOI waveguide with propagation loss as low as 1.2 dB/mm. Examples of SOI optical waveguide devices are also presented, such as sharp bends and ring resonators with a quality factor larger than 50,000.

Keywords: inductively coupled plasma (ICP) etch, Silicon-on-insulator (SOI), electron-beam lithography (EBL), waveguides, propagation losses.

1. INTRODUCTION

Silicon-on-insulator (SOI) is transparent at telecom wavelength, which provides a good platform for dense integration of optical devices. SOI submicrometer optical waveguides and the related passive components are essential for building more complex devices compactly. These devices promise to play important roles in future applications of opto-electronic signal processing and telecommunications. As the dimension scales down, the fabrication of photonic waveguide and construction of photonic integrated circuits (PIC) become a problem. Therefore, a good processing technology is required to transfer the pattern accurately and diminish the sidewall roughness.

In this paper, both strip and rib waveguides are fabricated using electron-beam lithography (EBL) and ICP dry etching, which are two main techniques in fabrication. In addition, the propagation losses of the waveguides are measured by using both cut-back and Fabry-Perot resonance methods at telecom wavelength. Based on these measured results, some functional components with small dimensions, including bends with radius of a few micrometers, microring resonator, and MMI couplers, are fabricated[1]. The functions of power splitter and bar or cross coupler are realized[2]. All of these components show great potential in silicon photonic integration circuits.

2. FABRICATION AND FABRICATION ISSUES

All of our devices were fabricated on UNIBOND SOI wafers provided by SOITEC. The thicknesses of top silicon layer and buried oxide (BOX) layer are 340nm and 1μm respectively. The fabrication process was as follows: Firstly PMMA (Polymethyl Methacrylate) resist was spin-coated on the SOI wafer. Then Raith150 electron beam lithography system was used to pattern the structures onto the resist layer. After developing and stopping, the top silicon was then etched down with an Alcatel 601E inductively coupled plasma (ICP) dry etcher. Finally the resist was stripped and the devices were cut from the wafer, facets were prepared by polishing or by etching and cleaving. As an optional step, an oxide top cladding layer was formed by PECVD deposition or thermal oxidation.

SOI etch was carried out on an Alcatel 601E etching tool and the pattern was transferred into the SOI wafer using a C_4F_8/SF_6 ICP process. This tool is fitted with a high density ICP type plasma RF source and a low frequency (LF)

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source. In the experiments, a mechanical clamping chuck was used to fix the wafer of 100 mm in diameter, which allows a wide range of wafer temperature during the etching process. Small chips were glued on an aluminum wafer or a silicon wafer coated by oxide.

2.1 Straight Waveguide

The waveguide width is 400 ~ 450 nm and the thickness of the slab layer is 140 nm, which satisfy the single-mode condition as predicted by rigorous full-vector film mode matching (FMM) simulation[3]. The simulated result of its fundamental mode profile is obtained. We analyze the effects of the geometrical parameters of the waveguides on their polarization characteristics. Finally the waveguide loss mechanisms are summarized and the effects of geometrical parameters, thickness of the buried oxide layer and roughness of sidewall on the transmission loss of the waveguides are analyzed. In this study, our concern is only focused on the roughness of the sidewall.

As the cross-sections of the waveguides scale down to submicrometer, electron beam lithography and ICP dry etching are used to fabricate the waveguides and devices. The main methods for reducing the sidewall roughness include reducing of the edge roughness of the resist pattern[4], optimization of dry etching process[5], thermal oxidation of sidewalls and etch-back, and anisotropic wet-etch[6]. In this study, we focus on optimizing the ICP etching parameters to obtain smooth sidewall, but in our opinion, the former method mentioned above is important than the latter.

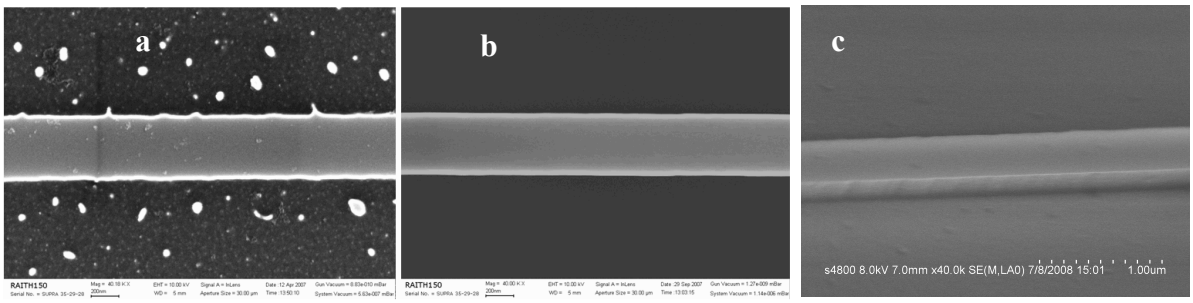

Fig. 1. SEM image of an SOI based waveguide. (a) result of etching a wafer with contamination and PMMA scumming , (b) result of etching a wafer with clean surface (well developed), (c) waveguide sidewall.

Fig. 1 shows the etching results of wafer pattern with different developing times. Fig. 1(a) presents a coarse bottom surface, whose roughness is induced by PMMA scumming. The line edge is also rough and it will transfer into the waveguide during etching. Fig. 1(b) is the top view and Fig.1(c) is the side view of a clean open area after etching.

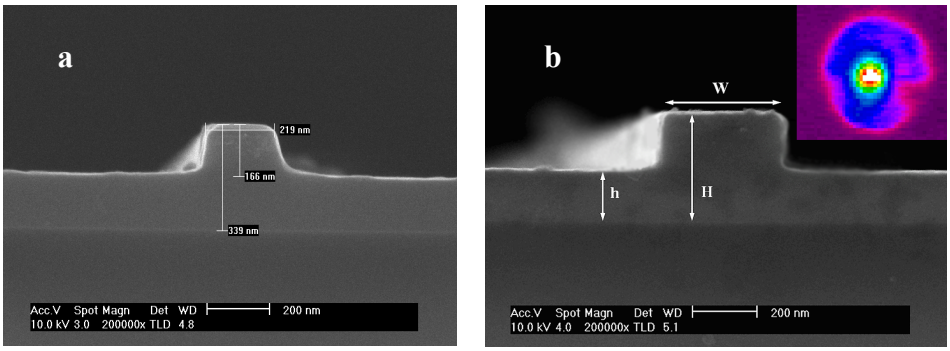

Fig. 2. SEM image of an SOI based rib waveguide. (a) positive profile, (b) vertical profile. Inset: the output light spot for quasi-TE mode.

Fig. 2 shows the profile of examples of SOI waveguide. Roughness surface, bad waveguide geometry, and also dimension shrink will induce scattering and loss. If the patterns were not well developed, the open areas will be coated by a PMMA film, which will cause bad geometry and dimension shrinking, even if O_2 plasma strip processing was adopted to remove the remaining PMMA film (Fig. 2(a)). In Fig. 2(b) we can see a better result. The facet was prepared by polishing. The Fabry-Perot resonance method showed that the propagation loss is about 1.59 dB/mm.

2.2 Waveguide bends

The most important advantage of photonic wire waveguides is that ultra compact bend with radius of few micrometers can be realized. We fabricated a lot of sharp 90° bends with different radii (3 μm, 5 μm, 10 μm, 20 μm, etc). We also measured the insertion loss of these bends with different radii. All the devices had eight 90° bends and a totally length of 1mm. The bend loss decreased exponentially as the bend radius increased. When the radius of the bend waveguides is 5μm and its bending loss is 0.14dB/90°. These ultra compact bends enable us integrate more devices into the wafer with small footprint.

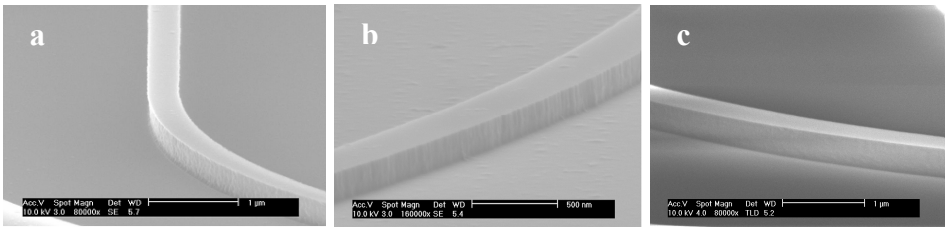

Fig. 3. SEM image of the bend strip waveguide. (a) Undercut induced by long time overetch. (b) PMMA shrinking caused by low selectivity, line edge roughness transferred to waveguide sidewall. (c) Low loss bend waveguide fabricated by optimized process.

Unlike the rib waveguide, Strip waveguide should be etched to the buried oxide (BOX) layer. **A**s soon as the oxide layer is reached, the etching chemistry balance would be broken, especially for a higher bias power. The overetching time must be under controlled, or will induce undercut in the sidewall as show in Fig. 3(a), and increasing the C_4F_8 ratio would reduce the undercut. As show in Fig. 3(b), if the bias power is too high and the pressure is low, PMMA line edge would shrink and its roughness would transfer to the sidewall clearly. To keep the design dimension and get a smooth sidewall, high selectivity is needed.

2.3 Facet Preparation

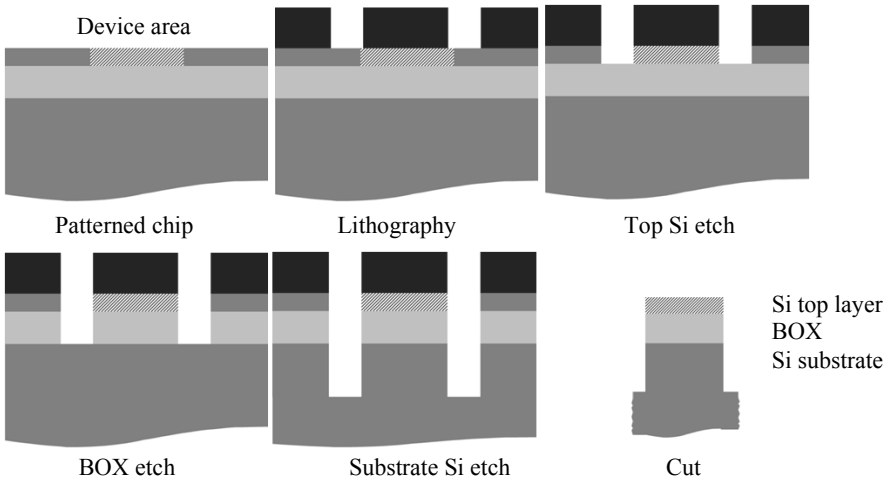

Fig. 4. Fabrication process for facet

Optical lithography and a series of ICP etch process were used to define the input/output facet. Compared with the facets prepared by polishing, the facets fabricated by etching are smooth and also have low scattering loss. By etching method all the facets in one wafer can be fabricated at once with few more processes and the device and waveguide length is well controlled.

After the PMMA mask to define the device is removed. A PR mask is spun on to define the facets, and then the top silicon layer, buried oxide (BOX) layer and substrate silicon will be etched in turn as illustrated in Fig. 4 “Bosch” process has been used in the substrate silicon deep etch. At the last etching process, a deep U-groove which makes cleaving easy was formed.

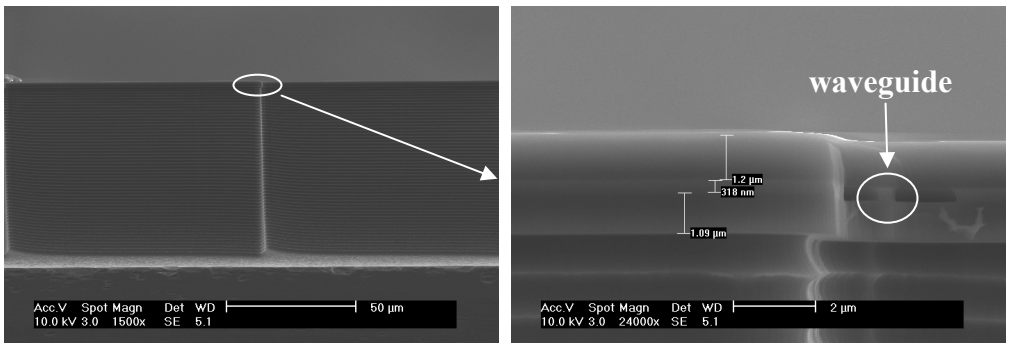

Fig. 5. SEM of the facet fabricated by optical lithography and ICP etching

The roughness of the facet prepared by etching is investigated using SEM picture. Fig. 5 presents an SEM imagine of a waveguide facet after a series of etching. In the waveguide, the facet exhibits a smooth surface without undercut or deformation.

3. FABRICATED STRUCTURES

The ICP etching process was optimized after a large number of experimental trials and the devices are fabricated. A high-performance microring resonator based on SOI rib waveguide has been realized.

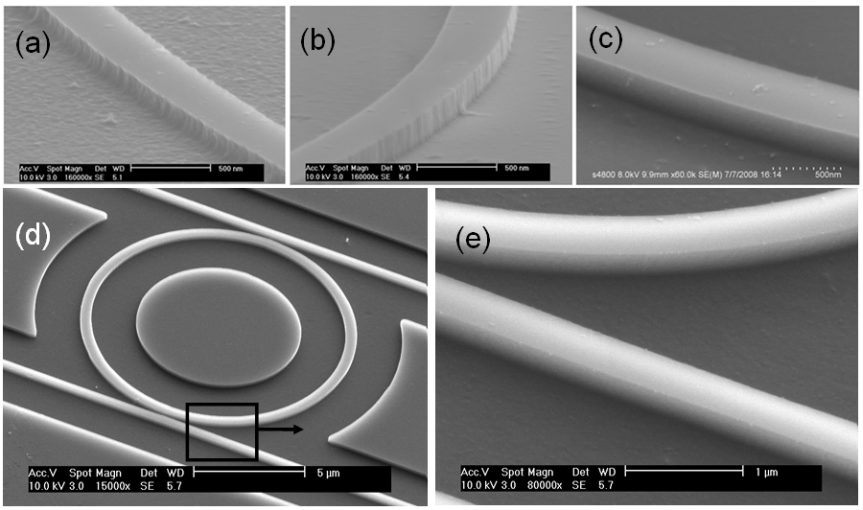

Fig. 6. SEM part images of microring resonator etched by different receipe

As shown in Fig.6, the splitting ratios of about 20 dB around 1550 nm were obtained for both polarizations at the drop port, with a quality factor of 53,000, and an extinction ratio of 14.0dB. Propagation loss in the ring is minimized, and a low propagation loss of 3.9dB/cm is demonstrated in a curved waveguide. Obviously, this high Q microring resonator is expected to lead to high speed optical modulators and bio-sensing devices.

Some other devices have also been fabricated, including SOI submicron waveguides, inverse taper, multimode interference (MMI) coupler, and Mach-Zehnder interferometer. These devices are measured on an auto-aligned fiber-waveguide-fiber measurement system. The measurement results show that we have demonstrated straight waveguides with transmission loss of 1.2dB/mm, bend waveguides with radius of 5µm and bending loss of 0.14dB/90°, inverse taper for fiber and rib waveguide with coupling loss of 2.1dB, MMI coupler with good power balance and low extra loss, and MZI filter with asymmetric arm length.

4. CONCLUSION

With cooperation of EBL, the sidewall roughness of the SOI sub-micron waveguide was reduced greatly by optimizing the ICP etching process. As a result, the propagation loss was diminished. Some SOI rib waveguide base elements were fabricated and the experimental results agreed well with the simulation results. Such fabrication processes also have been used in photonic crystal waveguides and high aspect ratio short period grating fabrication. While detailed process characterization and development is required, smooth sidewalls and perfect geometry is needed to improve the characteristics of SOI waveguide based devices.

ACKNOWLEDGMENTS

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