

The Application of Ion-Beam Mixing, Doped Silicide, and Rapid Thermal Processing to Self-Aligned Silicide Technology

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ABSTRACT

In this paper we have developed a SALICIDE process for CMOS applications using ion-beam mixing for silicide formation and doped silicide in conjunction with RTA drive-in for shallow silicided junction formation, and have investigated the fundamental issues related to this process. Specifically, we have studied (i) the effects of ion-beam mixing and RTA on the properties of Ti SALICIDE and the interaction between Ti and SiO_2 ; (ii) the self-aligned $\text{TiN}_x\text{O}_y/\text{TiSi}_2$ formation and phase transformation; (iii) the mechanism of impurity redistribution and segregation, and junction formation during RTA drive-in; and (iv) the performances and reliability of fabricated SALICIDE devices. Results show that this process may have a great impact on future VLSI technology.

INTRODUCTION

As the size of MOSFET devices decreases, the RC time delay due to the wiring that is used to contact the device gate, source, and drain, does not scale with the shrinking of the physical dimensions of the device. Therefore, for scaled-down MOSFETs, the RC speed enhancement can be compromised by the time delay due to the wiring. The self-aligned silicide (SALICIDE) technology, in which silicides are formed simultaneously on source/drain and diffused interconnects with the gate, has received much attention [1-3]. Among metal silicides considered for SALICIDE technology, titanium silicide has been the most promising one because of its low resistivity, good adhesion, high temperature stability, and the capability of dissolving the native oxide on the silicon surface upon annealing.

Using the conventional SALICIDE process for CMOS applications has several problems, including native oxide at the metal/Si interface which slows down the reaction and results in a rough silicide surface, critical ambient control, lateral silicide growth, and non-ohmic contacts due to significant dopant redistribution during silicide formation. The native oxides at the Ti/Si interface cause the reaction to proceed in a non-uniform fashion, resulting in a rough silicide surface. It has also been reported that a high concentration impurity such as As at the Ti/Si interface retards titanium silicide formation. Therefore, the growth rates of titanium silicides formed on n^+ (As doped) and p^+ (B doped) regions are different, resulting in different amounts of silicon consumption on the diffusion regions of p- and n-channel MOS devices. Furthermore, significant dopant redistribution on source and drain areas occurs during SALICIDE formation, which makes the ohmic contact very difficult.

To solve these problems we have developed a novel SALICIDE technology using rapid thermal annealing and ion-beam induced interface mixing techniques for self-aligned Ti silicide formation, and a doped silicide technique for shallow junction formation. The detail structure and process steps of this technology are shown in Fig.1. After polysilicon gate patterning and oxide spacer formation, a layer of titanium was sputter

deposited on the wafers. These wafers were then implanted with $^{28}\text{Si}^+$ ions to achieve interface mixing. The wafers were then first annealed at a relatively low temperature in a nitrogen ambient using RTA. The titanium nitride and unreacted Ti were then selectively removed followed by a high temperature RTA in a NH_3 ambient for contact barrier formation. Suitable impurity ions are then implanted into silicide layers for shallow silicided junction formation. After the BPSG deposition, high temperature RTA is used to drive-in the implanted ions from the silicide layers into the Si substrate as well as anneal the BPSG layer, followed by contact opening, Al sputtering and sintering.

In general, this technology has several significant advantages over other techniques including enhanced Ti-Si reaction rate, improved surface morphology, and smoother silicide/Si interfaces due to the suppression of the native oxide effects at the Ti/Si interface, same silicide thicknesses formed on both n- and p-channel devices, reduction in lateral silicide growth, and better ambient control. In addition, since dopants are implanted into the silicide layer instead of the Si substrates, no implantation damage is created in the Si substrates for shallow junction formation. By controlling the subsequent RTA drive-in conditions, it is possible to achieve silicided shallow junctions with sufficiently high carrier concentration at the silicide/Si interface for ohmic contacts.

EXPERIMENTAL

The starting specimens were 5" p-type Si wafers of 14 - 22 $\Omega\text{-cm}$ resistivity and (100) orientation. Ti films of 750 Å in thickness were sputter deposited on the wafers. The as-deposited films had a sheet resistance of $\sim 9 \Omega/\text{square}$. These wafers were then implanted with $^{28}\text{Si}^+$ ions at 85 - 100 keV to a dose of $1\text{E}15\text{-}1\text{E}16$ to achieve interface mixing. The wafers were then first annealed at 650°C for 30s in N_2 using RTA. The TiN and unreacted Ti were then selectively removed in a chemical solution of H_2O_2 , NH_4OH , and H_2O mixture with a volume ratio of 1 : 1 : 5, followed by a high temperature RTA in NH_3 or N_2 for TiN contact barrier formation as well as sheet resistance reduction.

We have fabricated various devices and test structures to study the fundamental issues related to this technology described above and examine the applicability of this technology to the submicron SALICIDE structure. These include diodes, capacitors with polycide gate, and MOSFETs with SALICIDE structure using doped silicide technology. In addition, test structures for contact resistance, sheet resistance, and lateral silicide growth measurements have been made. Extensive measurements using spectroscopic techniques, such as SEM, XTEM, TED, SIMS, RBS, XRD, ESCA, XPS, and AES were made to study the structure and chemical properties of materials and devices.

RESULTS AND DISCUSSION

Ion-Beam Mixing

The effect of the interface native oxide contamination can

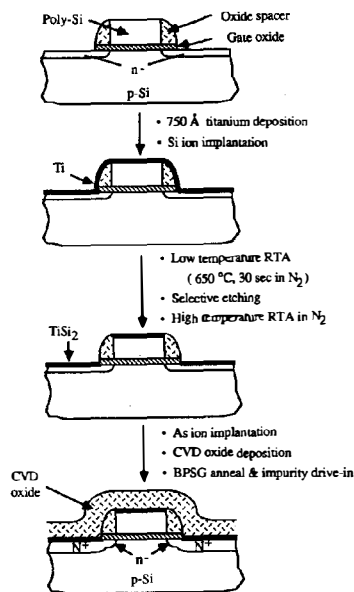


Fig.1 Structure and process steps of a SALICIDE process using ion-beam mixing, doped silicide, and RTA

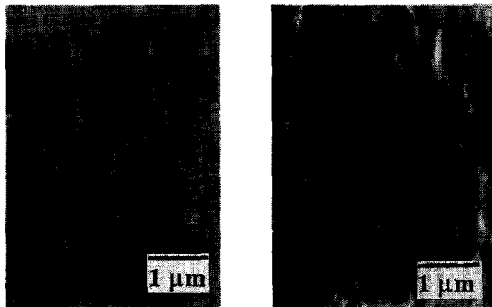


Fig.2 SEM surface morphology of TiSi_2 formed on single crystal Si (a) with and (b) without ion-beam mixing

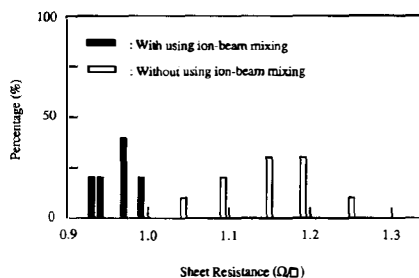


Fig.3 Effect of ion-beam mixing on sheet resistance and uniformity of Ti SALICIDE. Ti thickness is 750 Å.

largely be suppressed by implanting ions through the deposited metal films on Si. The ion-beam mixing breaks up the oxide at the Ti/Si interface and achieves interface mixing that enhances the Ti-Si reaction rate and results in a smooth silicide surface. We have studied TiSi_2 formation by ion-beam mixing and RTA, with primary focus on uniform TiSi_2 formation and lateral silicide growth reduction. TiSi_2 surface morphology, sheet resistance uniformity, effects of Si implantation on Ti/ SiO_2 interaction, and lateral growth problems were investigated. Isolation between the gate and source/drain of SALICIDE 1- μm MOSFETs fabricated using this technology was also examined.

One of the major advantages of using ion-beam mixing is the improvement of surface morphology. Fig. 2 shows the surface morphology of TiSi_2 formed on single crystal Si (a) with and (b) without ion-beam mixing. It is evident that the surface morphology is significantly improved by the use of ion-beam mixing. In addition, ion-beam mixing results in better resistivity uniformity, as shown in Fig. 3.

To implement ion-beam mixing technique into the SALICIDE process, it is of crucial importance to examine the Ti- SiO_2 interaction. During the SALICIDE process, the field and spacer oxides are subjected to interaction with Ti. Any interaction between Ti and SiO_2 that leaves any residue on the oxides could cause bridging between the gate and source/drain. From the ternary phase diagram of the Ti-O-Si system, the most possible stable phases for thin Ti films deposited on thick oxide layers are Ti_2O_3 , SiO_2 , and Ti_5Si_3 if Ti- SiO_2 interaction takes place. To investigate the effects of Si ion implantation on the Ti- SiO_2 interaction, samples with Ti deposited on either CVD oxides or thermal oxides on Si were prepared. Fig. 4 shows the XPS spectra taken from these samples with thermal oxides (a) and CVD oxides (b) after Si implantation at a dose of 1×10^{16} , low temperature RTA and selective etch. As illustrated in the enlarged spectra, that within the experimental limits no $\text{Ti}(\text{2P}_{3/2})$ peaks were detected. This implies that Ti and its compounds, such as TiN , Ti oxides, and Ti silicides, were not left on the surface of either thermal or CVD oxides, indicating that ion-beam mixing even with a very heavy dose does not enhance the interaction between Ti and oxides.

It is known that during titanium silicide growth, Si is the dominant moving species. Since the lateral growth is a diffusion controlled process, the use of ion-beam mixing and RTA can further reduce the probability of lateral silicide growth. Samples with patterned polysilicon on SiO_2/Si and with LOCOS isolated single-crystal Si were used to study the lateral silicide growth. Both XTEM and SEM micrographs of these structures indicate no silicide lateral growth has been observed on SiO_2 at the edge of the structure after SALICIDE process. The measurements of leakage current between gate and source/drain of SALICIDE MOSFETs fabricated using ion-beam mixing and RTA are shown in Figs. 5(a) and (b). It is evident that negligible conduction between gate and source/drain for applied voltages of up to 17 V is obtained, indicating good control of lateral silicide growth.

Self-aligned $\text{TiN}_x\text{O}_y/\text{TiSi}_2$ Contact Formation

It has been shown that the Al/ TiSi_2 /Si contact system is not thermally stable [8]. Electrical measurements on shallow junctions with Al/ TiSi_2 /Si contacts show that the diodes are all shorted after annealing at 400°C for 30 min due to the Si and Al interdiffusion through the TiSi_2 . To improve contact reliability, TiN has been used as a contact barrier and the Al/TiN/ TiSi_2 /Si contact system has significantly improved thermal and electrical stabilities. We have prepared self-aligned $\text{TiN}_x\text{O}_y/\text{TiSi}_2$ layers on contact areas during the SALICIDE process by direct RTA of TiSi_x in NH_3 for contact barrier formation [6]. The thickness ratio of $\text{TiN}_x\text{O}_y/\text{TiSi}_2$ layers is controlled by RTA temperature and/or time used. The simplicity of the process and the lower

temperature and/or shorter time used for TiN formation make it very attractive for submicron MOS device applications.

The TED analysis of the film after 1st RTA and selective etching indicates that the film consists mainly of a TiSi phase and some traces of a TiSi₂ phase. The 2nd RTA, performed at higher temperatures in NH₃, converted the surface of the silicide layer into TiN and TiSi₂. The TED pattern and TEM micrograph of the sample which received the 2nd RTA at 900°C for 10 sec in NH₃, indicate that the film consists of three phases: TiN fcc phase, TiO fcc phase, and stable C₅₄ TiSi₂ face-centered orthorhombic phase. These results were also verified by RBS analysis. Fig. 6 shows the RBS spectra of the films after 2nd RTA in NH₃ or in N₂. For the sample annealed in NH₃, the film consists of two layers and the signals from N and O are clearly visible. However, a negligible amount of TiN was found in the N₂ annealed sample as compared with that in the NH₃ annealed one, contrary to the results reported in Ref. 7. The XTEM of the bilayer formed by this method (1000°C, 10s) in NH₃ clearly shows the bilayer formed on top of the silicon substrate. The sheet resistance of the sample as a function of process steps is shown in Fig. 7. It drops from ~8 Ω/square to ~3 Ω/square after selective etching because of the formation of TiSi in the film. After bilayer formation, it drops again to ~1.45 Ω/square. The film has been converted completely to a TiN/TiSi₂ bilayer. Moreover, the existence of O in the form of titanium oxide on the surface of the top layer has been observed by AES and RBS. Therefore, a more appropriate description of this bilayer would be TiN_xO_y/TiSi₂.

The chemical stability of TiN_xO_y/TiSi₂ in dilute HF (20:1) was studied by measuring the sheet resistance change. The sheet resistance of TiN_xO_y/TiSi₂/Si does not change at all in dilute HF for at least 60 s. This indicates that TiN_xO_y formed by direct RTA of TiSi+TiSi₂ in NH₃ has good chemical stability in dilute HF. On the contrary, the film which received 2nd RTA in N₂ shows a poor chemical stability in dilute HF. The sheet resistance increased immediately and dramatically after dipping the sample into the dilute HF solution.

The contact barrier properties of TiN_xO_y formed by RTP on TiSi₂/Si were studied by investigating the interdiffusion of 300 nm Al and Si in the Al/TiN_xO_y/TiSi₂/Si system as a function of sintering conditions. The Al sintering was carried out in forming gas for 30 minutes at different temperatures ranging from 400°C to 550°C in 50°C increments. Auger depth profiles of each layer after Al deposition and after sintering at 500°C for 30 minutes are identical. Serious interdiffusion occurs after the 550°C sintering and XRD spectrum reveals the presence of a ternary compound of composition Ti₇Al₅Si₁₂. After removing Al, TiN_xO_y, and TiSi₂ layers sequentially from the sample sintered at 500°C for 30 minutes, the integrity of the contact system was studied using SEM. Compared with Si surface of the unannealed sample, no pin holes were observed on the Si surface. From these results we can conclude that the Al/TiN_xO_y/TiSi₂/Si contact system has good thermal stability up to 500°C, for 30 minutes sintering.

Boron Diffusion in SiO₂/TiSi₂/Si Structure and Shallow p⁺-n Junction Formation

Shallow junctions with a high surface carrier concentration are required to reduce the short-channel effects and form the ohmic contact. However, the shallow junctions cause an increase in sheet resistance on diffusion areas and result in a high contact resistance. The use of silicide on diffusion areas is, therefore, necessary to reduce the contact resistance in submicron device fabrication. However, the growth rates of TiSi₂ on n⁺ and p⁺ regions are different [4,5] because As at the Ti/Si interfaces retards the TiSi₂ formation. Another major concern is the dopant loss during silicide formation. Without oxide capping, a significant loss of dopant (70-75% of As and ~90% of B) in the source/drain regions was observed [9]. Both arsenic and boron

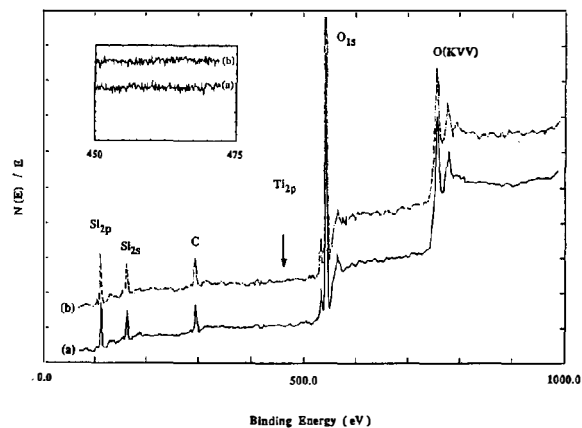


Fig.4 XPS spectra of the surfaces of (a) thermal oxides and (b) CVD oxides after Si implant (1E16), low temperature RTA in N₂, and selective etching

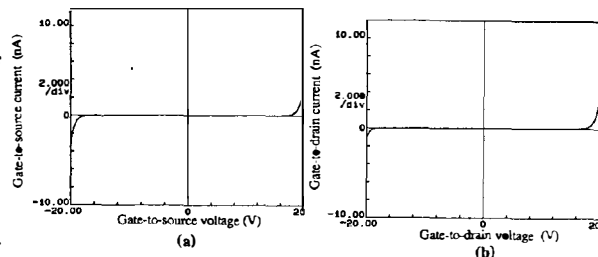


Fig.5 Leakage current measurements of (a) gate-to-source and (b) gate-to-drain of MOSFets with Ti SALICIDE structure fabricated using ion-beam mixing and RTA.

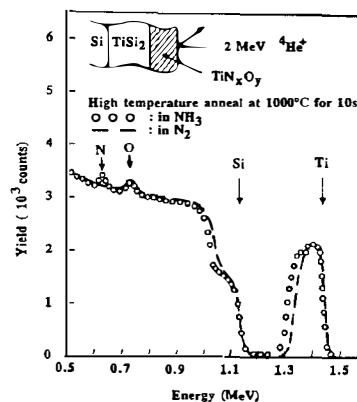


Fig.6 RBS spectra of Ti/Si after low temperature RTA (650°C, 30 sec) in N₂, selective etching, and high temperature RTA (1000°C, 10 sec) in NH₃ or N₂.

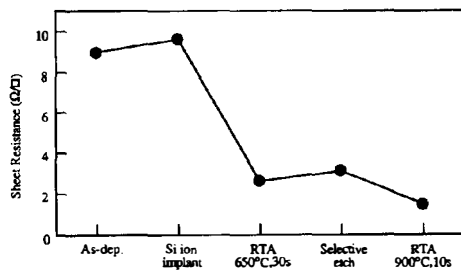


Fig. 7 Sheet resistance of Ti on Si as a function of SALICIDE process steps

diffuse into the silicide layer, which exhibits the double peaks with the first peak at the TiSi_2/Si interface and the second at the TiSi_2 surface. Even for samples with oxide capping to prevent dopant evaporation, a significant portion of the dopant was lost from the Si substrate to the silicide or oxide layers. The primary mechanism of dopant redistribution appears to be snowplow into the Ti-rich region ahead of forming silicide at the initial silicide formation temperature (500-700°C). At high temperature RTA, the loss of dopants is significant. Therefore, shallow junctions with high surface carrier concentrations can hardly be obtained.

Recently, diffusion of dopants from the doped silicide layer on Si into the Si substrate has been shown to be a very promising technique for the formation of silicided shallow junction with high surface carrier concentration at the silicide/Si interface. As compared with other methods, the doped silicide technique has these advantages: (i) the silicide layer is formed before junction formation, which produces the same silicide thickness on both n- and p-channel devices; (ii) junction depth is controlled by the drive-in annealing temperature and/or annealing cycle; and (iii) no implantation damage in the substrate is created.

In this work, shallow silicided junctions have been formed by implanting boron ions into silicide layers and the subsequent drive-in of the implanted ions into the Si substrate during high temperature RTA. Ti films of 110 nm in thickness were sputter deposited on N-type (100), 2 - 6 Ω-cm Si wafers after standard cleaning procedures. These wafers were first annealed at 950°C for 70 s in N_2 to form TiSi_2 . The TiN layer over the TiSi_2 film was then selectively removed. The measured thickness of the TiSi_2 film was ~2500 Å. After depositing 1500 Å CVD oxide films on TiSi_2 , the wafers were then implanted with boron ions at 50 keV to a dose of $1\text{E}15$ to $1\text{E}16$. The subsequent drive-in was carried out using RTA at a temperature between 900°C and 1100°C for 30 s in N_2 . The boron diffusion in TiSi_2 , shallow junction formation, and boron redistribution at $\text{SiO}_2/\text{TiSi}_2$ and TiSi_2/Si interfaces were investigated using SIMS.

P-channel 1 μm LDD MOSFETs with SALICIDE structures were fabricated and their electrical characteristics were studied. P regions were implanted with BF_2 ions of 40 keV to a dose of $1\text{E}13$. After Ti SALICIDE formation (~1500 Å) and 200 nm oxide deposition, boron ions at energy of 40 keV to a dose of $7.5\text{E}15$ were implanted into TiSi_2 as a source for p^+ formation. p^+/n diodes of $1 \times 10^{-3} \text{ cm}^2$ were also formed during the above process. The drive-in process was carried out simultaneously with BPSG anneal (900°C, 20 sec in N_2 by RTA).

As shown in Fig. 8, most of the boron ions were implanted into the TiSi_2 layer, while only ~1.1 % of them were implanted into the underlying Si substrate. After RTA, some of the boron ions in the TiSi_2 layer diffused into the Si substrate. A 0.2 μm p^+/n junction with a surface concentration of $1 \times 10^{20} \text{ cm}^{-2}$ at the TiSi_2/Si interface was obtained by RTA at 900°C for 30 sec with a boron dose of $1\text{E}16$. Meanwhile, about 25 % of the boron has piled up at the $\text{SiO}_2/\text{TiSi}_2$ interface. In addition, the amount of boron atoms at the $\text{SiO}_2/\text{TiSi}_2$ interface increases, being more

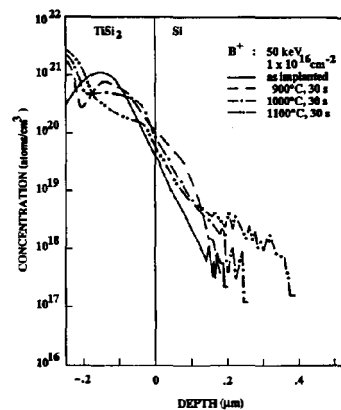


Fig. 8 SIMS data of boron diffusion profiles in $\text{SiO}_2/\text{TiSi}_2/\text{Si}$ structure after RTA drive-in anneals.

pronounced at higher RTA drive-in temperatures. The ratio of boron piling up at the $\text{SiO}_2/\text{TiSi}_2$ interface increases from ~25% for RTA drive-in at 900°C to ~44 % at 1000°C and to ~79 % at 1100°C. However, no boron pile-up was observed at the TiSi_2/Si interface. The lack of pile-up of boron at the TiSi_2/Si interface makes the ohmic contact formation difficult and sets up a limit for the drive-in temperature. The estimated diffusion coefficient of boron in TiSi_2 is in the range of 10^{-12} to $10^{-11} \text{ cm}^2/\text{s}$ at temperatures between 900°C and 1100°C. This value is about 2 to 3 orders of magnitude higher than that observed in the same temperature range in single crystal silicon (10^{-15} - $10^{-13} \text{ cm}^2/\text{s}$).

Similar to boron diffusion in the $\text{SiO}_2/\text{WSi}_2/\text{Si}$ structure [10], there is a new phase (boron precipitation) that continues to grow at the $\text{SiO}_2/\text{TiSi}_2$ interface as the annealing process proceeds. During the growth of this new phase, more and more boron was attracted to the $\text{SiO}_2/\text{TiSi}_2$ interface. From the TED of the TiSi_2 surface layer near the $\text{SiO}_2/\text{TiSi}_2$ interface after RTA drive-in, the boron precipitation at the $\text{SiO}_2/\text{TiSi}_2$ interface is identified as the hexagonal B_2O_3 phase. The continuous growth of this precipitating phase results in an attraction source for boron diffusion towards the $\text{SiO}_2/\text{TiSi}_2$ interface.

The X-TEM micrograph of the annealed $\text{SiO}_2/\text{TiSi}_2/\text{Si}$ structure reveals a very high crystal quality of the shallow p^+/n junction formed by doped silicide technology. The leakage current of the diode at a reverse bias of 5 V is less than 3 pA ($3 \text{ nA}/\text{cm}^2$) and the ideality factor is ~1.02. P-channel MOSFETs ($L/W=1/25$) with well behaved I-Vs have been fabricated using doped silicide technology.

Device Performance and Reliability

The effects of ion-beam mixing on diode leakage current and device characteristics of MOS capacitors and short channel NMOSFETs under constant current stress and hot carrier stress were examined. N-channel SALICIDE (Ti thickness = 750 Å) LDD MOSFETs ($W/L=50\mu\text{m}/1.2\mu\text{m}$) with 250 Å gate oxide were fabricated on p-type (100) Si wafers with resistivities of 14 - 22 Ω-cm. Ion-beam mixing was done with $1\text{E}15$ Si ions at 85 keV. After 1st RTA, As ions at a dose of $5\text{E}15$ were implanted into the TiSi_2 layer as a source for subsequent n^+ region formation. Polycide gate MOS capacitors with an area of $4 \times 10^{-4} \text{ cm}^2$ as well as p-n junction diodes of $1 \times 10^{-3} \text{ cm}^2$ were also formed during the above process. The drive-in of implanted ions into the Si substrates was carried out simultaneously with the BPSG anneal (900°C, 20s in N_2). For comparison, devices with SALICIDE structure but without using the ion-beam mixing technique were also fabricated.

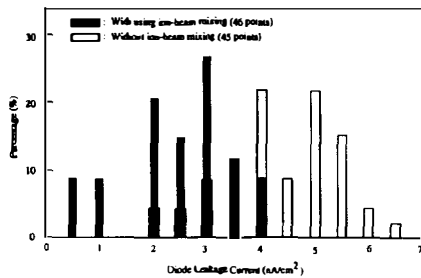


Fig.9 Comparison of leakage current distribution between junctions made with and without ion-beam mixing

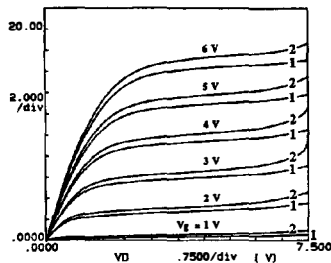


Fig.10 I-V characteristics of LDD NMOSFETs (W/L=50/1.2) fabricated with Ti SALICIDE (1: with ion-beam mixing, 2: without ion-beam mixing).

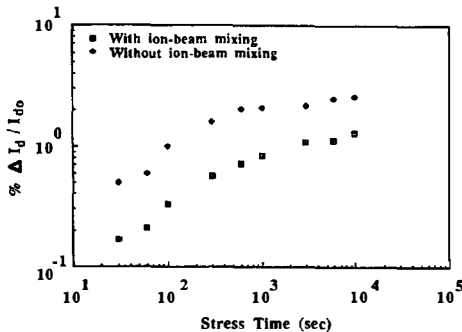


Fig.11 Degradation of the drain current in the linear region of LDD NMOSFETs fabricated using Ti SALICIDE.

Measurements on junction leakage currents of p^+n diodes on 5" wafers at a reverse bias of -5 volts show that ion-beam mixing results in smaller junction leakage current and tighter distribution, as shown in Fig. 9. The lower leakage current and tighter distribution observed in ion-beam mixed samples is attributed to the better $TiSi_2/Si$ interfaces. For MOS devices, charge trapping in the gate oxide under external stress has a strong influence on oxide failure and long term device reliability. Our results indicate no significant difference in dielectric strength among different sample splits. Measurements on the gate voltage shifts required to maintain a gate current density of 2.5 nA/cm^2 under constant current stress indicate that MOS capacitors fabricated with Ti SALICIDE using ion-beam mixing presents less gate voltage shift as compared with that fabricated without using it. This means that the electron trapping is less in ion-beam mixed samples due to the stress relief in the polycide gate.

The I-V characteristics of n-channel LDD MOSFETs are shown in Fig. 10. The thickness of the Ti SALICIDE (1600Å)

formed with using ion-beam mixing is thicker than that (1300Å) formed without using it. Since the same impurity dose, implant energy, and drive-in RTA were used to form a shallow junction in both cases, a deeper junction depth can, therefore, be expected for n-channel MOSFETs fabricated without using ion-beam mixing and, thus, result in a higher current drive capability. Although ion-beam mixing reduces the current drive of SALICIDE devices, it leads to improvement on other device characteristics such as smaller subthreshold slope, smaller SiO_2/Si interface state density, and higher drain breakdown voltage. The ion-beam mixing reduces the subthreshold slope from 93 mV/decade to 89 mV/decade, implying a reduction of interface state density at the SiO_2/Si interface.

Hot carrier stress was performed at peak substrate current condition ($V_g=3 \text{ V}$, $V_d=7 \text{ V}$) to examine the effects of ion-beam mixing on device reliability. Fig. 11 shows the degradation of the drain current in the linear region of two SALICIDE MOSFETs $W/L = 50 \mu\text{m}/1.2 \mu\text{m}$ under hot carrier stress. Although both devices show very small degradation up to 10^4 sec , the one which received ion-beam mixing shows better resistance to hot carrier degradation. During the stress, no changes in threshold voltage or transconductance were observed for either device. The improved hot carrier resistance of ion-beam mixed devices could also be attributed to the better quality of SiO_2/Si interfaces.

CONCLUSION

In summary, we have developed a SALICIDE process for CMOS technology using ion-beam mixing for silicide formation and doped silicide in conjunction with RTA drive-in for shallow silicided junction formation, and have investigated fundamental issues related to this process. Specifically, we have studied (i) the effects of ion-beam mixing and RTA on properties of Ti SALICIDE and the interaction between Ti and SiO_2 ; (ii) the self-aligned $TiN_xO_y/TiSi_2$ formation and phase transformation; (iii) the mechanism of impurity redistribution and segregation, and junction formation during RTA drive-in; and (iv) the performance and reliability of fabricated SALICIDE devices.

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