

## Improvement of the Light Output Power of GaN-Based Vertical Light Emitting Diodes by a Current Blocking Layer

Hwan Hee Jeong, a,b Sang Youl Lee, Young Kyu Jeong, Kwang Ki Choi, June-O Song, Yong-Hyun Lee, and Tae-Yeon Seong, Kwang Ki Choi, Lee, a Young Kyu Jeong, Kwang Ki Choi, a June-O Song, Yong-Hyun Lee, b and Tae-Yeon Seong, Kwang Ki Choi, a June-O Song, a Young Kyu Jeong, a Kwang Ki Choi, a June-O Song, a Young Kyu Jeong, a Kwang Ki Choi, a June-O Song, a Young Kyu Jeong, a Kwang Ki Choi, a June-O Song, a Young Kyu Jeong, a Kwang Ki Choi, a June-O Song, a Young Kyu Jeong, a Kwang Ki Choi, a June-O Song, a Young Kyu Jeong, a Kwang Ki Choi, a June-O Song, a Young Kyu Jeong, a Young

<sup>a</sup>LG Innotek, Department of LED Business, Chip Development Group, Gwangju 506-251, Korea

The light output characteristics of GaN-based vertical light emitting diodes (1  $\times$  1 mm) fabricated by the multifunctional bonding material system have been investigated as a function of the linewidth of a SiO<sub>2</sub> current blocking layer (CBL). As the CBL width increases from 0 to 20  $\mu$ m, the forward voltage increases from 2.82 to 2.88 V at 350 mA, whereas the reverse leakage current decreases from  $4.90 \times 10^{-7}$  to  $3.05 \times 10^{-7}$  A at -10 V. The output power increases with increasing CBL linewidth. Furthermore, the output power of all the samples continuously increases without saturation across the current range of 0–1000 mA. © 2010 The Electrochemical Society. [DOI: 10.1149/1.3407625] All rights reserved.

Manuscript submitted March 16, 2010; revised manuscript received April 1, 2010. Published April 27, 2010.

GaN-based light emitting diodes (LEDs) are of considerable importance for applications in displays and solid-state lighting. In particular, for general illumination application, the optimization of larger chip area and higher driving current is essential. Conventional GaN-based lateral-type LEDs were known to be unsuitable for solid-state lighting applications because they suffer from poor heat dissipation and current spreading. 1-3 Thus, to solve the problems, the vertical-type LED configuration has been developed.<sup>5-8</sup> For verticaltype configuration, the laser lift-off (LLO) and chemical lift-off methods have been used to separate LED epitaxial layers from the sapphire substrate, which were then transferred to electrically and thermally conducting metal supporters. For example, Huang et al., investigating high power GaN-based vertical LEDs, reported that the vertical LEDs fabricated with a textured n-GaN surface produced 65% higher extraction efficiency compared to conventional GaN-based LEDs at an injection current of 20 mA. Wang et al. 10 fabricated vertical-structure metallic-substrate GaN-based LEDs by combining the electroplating process with a patterned LLO technique. Compared to conventional lateral LEDs, the vertical LEDs gave higher current spreading ability, larger extraction efficiency, and smaller forward voltage drop. Recently, our group also reported on the fabrication of 2 in. wafer level GaN-based vertical LEDs by employing a multifunctional bonding material system, which is composed of a thick Cu diffusion barrier and a bonding layer. Fully packaged vertical LEDs fabricated with an indium tin oxide (ITO)/AgCu contact by the bonding material system gave an operating voltage of 3.35 V at 350 mA. Even after over 1800 h, the operating voltages remained stable and the reverse currents were slightly increased to  $3-8 \times 10^{-7}$  A at -5 V.

The output power performance of lateral LEDs was significantly improved by minimizing current crowding around the p-pad electrode and photon absorption. <sup>12-14</sup> Current crowding results in an irregular and segregated light emission, lowering the luminous luminance efficiency of LEDs. Thus, to reduce the injection current underneath the opaque p-pad electrode, different methods were employed. For example, Huh et al. <sup>12</sup> introduced an insulating SiO<sub>2</sub> current blocking layer (CBL) beneath the p-electrode and showed that the external quantum efficiency of lateral LED chips with a CBL was significantly increased compared to those for the conventional LED chips. Liu et al., <sup>13</sup> also investigating a Ni catalytic process to form a high resistance region under the p-electrode, showed that the use of the selective activation resulted in about 15% increase in the light-output power compared to conventional LEDs. For vertical LEDs, recently, Uang et al. <sup>7</sup> introduced a SiO<sub>2</sub> CBL beneath the n-pad electrode, where the CBL was formed by induc-

tively coupled plasma (ICP) etching and plasma-enhanced chemical vapor deposition (PECVD) processes. They showed that the insertion of the CBL was very effective in improving the light output power of vertical LEDs. In this work, we have investigated the electrical and optical properties of wafer level fabricated GaN-based vertical LEDs as a function of the width of the SiO<sub>2</sub> CBL. In this work, the CBLs are not defined by an ICP etching process. The results show that the use of the CBL is fairly effective in improving the light output power, which increases with increasing linewidth of the CBL.

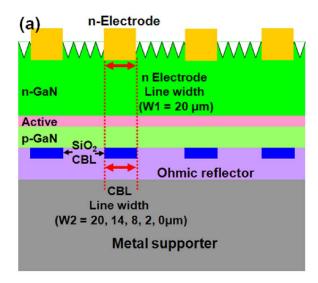
GaN-based epilayer stacks for vertical-type configuration LEDs were grown on (0001) sapphire substrate by metallorganic chemical vapor deposition. The LED epilayer stacks consisted of a 30 nm thick GaN nucleation layer, a 3 µm thick undoped GaN layer, and a 2 μm thick Si-doped n-GaN layer, an active region with seven periods of InGaN/GaN multiquantum wells (MOWs), 0.1 µm thick Mg-doped AlGaN, and a 0.2 µm Mg-doped p-GaN layer. The device fabrication steps were as follows: First, the samples were immersed into boiling aqua regia (HCl:HNO<sub>3</sub> = 3:1) for 10 min and then rinsed in running deionized (DI) water. Before lithography, the samples were ultrasonically degreased using acetone, methanol, and DI water for 5 min in each step followed by N<sub>2</sub> blowing. After the cleaning process, a square mesa structure  $(1 \times 1 \text{ mm})$  was fabricated using an ICP etcher for electric current isolation. The ICP process was used to etch away the p-GaN, MQWs, and n-GaN to expose the sapphire surface. A SiO<sub>2</sub> passivation layer was deposited by PECVD. Before the deposition of reflectors, CBLs were defined by photoresistor patterning on the p-GaN surface using the standard photolithographic and wet-etching processes, where the vertical centers of the CBLs and the n-pad electrodes were aligned, as shown in Fig. 1a. The CBLs varied from 8 to 20  $\,\mu m$  in width. After that, an ITO (50 nm) contact layer and a AgCu (200 nm) (2 atom % Cu) reflective layer were then deposited on the p-GaN layer by radiofrequency magnetron sputtering and electron-beam (E-beam) systems, respectively. After annealing, 50 nm thick Ti (an adhesion layer) and 1 µm thick Cu layers were deposited onto the AgCu reflective layer. A bonding metal alloy, consisting of Au, Sn, and Cu, was then deposited on the Ti/Cu layer by a dual E-beam system. This was followed by the deposition of a Ti layer onto the p-Si wafer, where the Ti metal was used as an ohmic contact layer to the p-Si wafer. After completing the LED structures, the whole wafer (2 in.) was bonded to the Si wafer by thermal compression at 300°C. An LLO process was then performed using an ArF excimer laser operated at a wavelength of 193 nm to separate the sapphire substrate from the LED structure, where an undoped GaN epilayer was exposed to air. The undoped GaN was etched to expose the n-GaN layer by wet chemical etching and ICP. A heated KOH solution was then used to roughen the n-GaN surface. A Cr/Al/Ti/Au film (ncontact) and a Ti/Au film (p-contact) were then deposited onto the

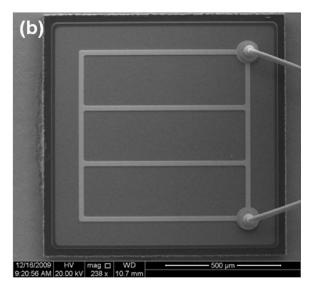
<sup>&</sup>lt;sup>b</sup>School of Electronic and Electrical Engineering, Kyungpook National University, Taegu 702-701, Korea

<sup>&</sup>lt;sup>c</sup>Department of Materials Science and Engineering, Korea University, Seoul 136-713, Korea

<sup>\*</sup> Electrochemical Society Active Member.

<sup>&</sup>lt;sup>z</sup> E-mail: tyseong@korea.ac.kr



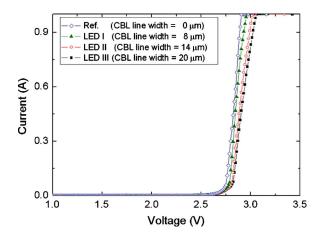


**Figure 1.** (Color online) (a) Schematic diagram of GaN-based vertical LEDs fabricated with CBL and (b) a plan-view optical micrograph of a vertical LED chip.

roughened n-GaN surface and the back surface of the p-Si wafer, respectively. Figure 1 illustrates the schematic diagram of GaN-based vertical LEDs fabricated with CBLs and a plan-view optical micrograph of the vertical LED chip. The linewidth of the n-contact electrode was fixed at 20  $\,\mu m$ , whereas the width of the CBL was 0 (referred to here as "Ref. LED"), 8  $\,\mu m$  (LED I), 14  $\,\mu m$  (LED II), and 20  $\,\mu m$  (LED III). To investigate the electrical, optical, and structural characteristics, the vertical LED chips (Fig. 1b) were encapsulated into standard LED lamps.

Figure 2 shows the typical forward current–voltage (*I-V*) characteristics of vertical LEDs as a function of the linewidth of the CBL. The forward voltages of Ref. LED, LED I, LED II, and LED III are measured to be 2.82, 2.83, 2.86, and 2.88 V, respectively, at an injection current of 350 mA. The forward voltage increases with increasing CBL width; Ref. LED shows the lowest forward voltage across the whole current range of 0–1 A. The forward voltages of all the samples slowly increase with increasing injection current up to 1 A. The finding that the LEDs with the narrower CBL give better electrical property could be attributed to an increase in the area for current flow and a reduction in the current conduction path.

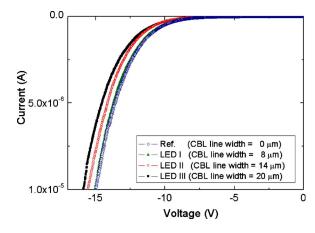
Figure 3 exhibits the typical reverse characteristics of the vertical LEDs as a function of the linewidth of the CBL. All the samples



**Figure 2.** (Color online) The typical forward *I-V* characteristics of vertical LEDs as function of the linewidth of the CBL.

give almost the same reverse current up to approximately -8 V. As the voltage exceeds -8 V, the reverse currents gradually increase. As the width of the CBL increases, the reverse leakage current decreases. For example, the reverse current of Ref. LED, LED I, LED II, and LED III are measured to be  $4.90\times10^{-7},\ 4.69\times10^{-7},\ 3.01\times10^{-7},\ and\ 3.05\times10^{-7}$  A, respectively at -10 V. The use of the CBL is effective in improving the reverse characteristics, indicating that the SiO<sub>2</sub> CBL serves as a passivation layer.

Figure 4 shows the light output power–current (*P-I*) characteristics of the vertical LEDs with and without the CBL. The output power increases with increasing linewidth of the CBL. The output powers of Ref. LED, LED I, LED II, and LED III are estimated to be 250, 264, 266, and 275 mW, respectively, at an injection current of 350 mA. LED III (namely, use of the CBL having the same width as that of the n-pad electrode) gives 10% improvement in the lightoutput power at 350 mA as compared to Ref. LED. The improvement could be attributed to a decrease in the vertical current under the n-pad electrode and an increase in the spreading current. This is consistent with the results previously reported by Kim et al., 14 showing that the relation between the vertical current under the n-electrode and the spreading current across the n-GaN layer was closely related to the electrical and optical performance of GaNbased LEDs. They showed that the increased vertical current resulted in lower light output power because most of the light emitted can be absorbed by the n-electrode. The output power of all the samples continuously increases without saturation across the whole current range of 0-1000 mA (Fig. 4). The appliance of high driving



**Figure 3.** (Color online) The typical reverse characteristics of the vertical LEDs as function of the linewidth of the CBL.

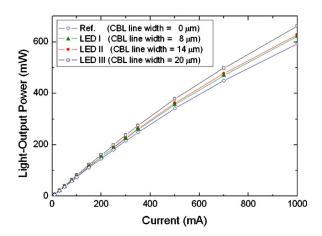


Figure 4. (Color online) The light output P-I characteristics of the vertical LEDs with and without the CBL

currents can cause a large reduction in the efficiency in GaN/InGaNbased LEDs, namely, the so-called efficiency droop. Different mechanisms have been proposed to describe the efficiency droop, including carrier leakage at high forward currents, <sup>15</sup> Auger recombination, <sup>16</sup> carrier overflow at high currents, <sup>17,18</sup> current leakage via structural defects, <sup>19,20</sup> carrier delocalization from In-rich low defect density regions, <sup>21</sup> and the effect of built-in piezoelectric fields in a quantum well. <sup>22</sup> Each of the mechanisms could only explain the electrical characteristics of related LEDs; there is no universal mechanism by which the efficiency droop in all different GaN/ InGaN-based LEDs can be clearly understood. The precise mechanism for the efficiency droop in our vertical LEDs remains to be further investigated. However, considering the fact that the overheating of an LED limits the output power, 17 the output power characteristics (Fig. 4) indicate that the multifunctionally bonded Si submount combined with the CBL might alleviate the droop effect by serving as effective current spreader and heat dissipater.

To summarize, we investigated the light output performance of GaN-based vertical LEDs (1  $\times$  1 mm) fabricated by the multifunctional bonding material system as a function of the linewidth of a SiO<sub>2</sub> CBL. As the width of the CBL increased, the forward voltage increased. However, the reverse leakage current decreased. The output power increased with increasing width of the CBL. The output power of all the samples continuously increased without saturation

across the whole current range of 0-1000 mA. The result indicates that the use of the CBL could represent a promising tool for fabricating high power GaN-based vertical LEDs.

This work was supported by LED Biz division of LG Innotek (LGIT) Co., Ltd. T.Y.S. is grateful to the Korea Science and Engineering Foundation (KOSEF) grant through World Class University program (R33-2008-000-10025-0) and the ERC/SRC Program (no. 2009-0064868) for the financial support.

Korea University assisted in meeting the publication costs of this article.

## References

- W. Y. Lin, D. S. Wuu, K. F. Pan, S. H. Huang, C. E. Lee, W. K. Wang, S. C. Hsu, Y. Y. Su, S. Y. Huang, and R. H. Horng, *IEEE Photon. Technol. Lett.*, 18, 1809 (2006).
- D. L. Hibbard, S. P. Jung, C. Wang, D. Ullery, Y. S. Zhao, H. P. Lee, W. So, and H. Liu, Appl. Phys. Lett., 83, 311 (2003).
- 3. B. S. Tan, S. Yuan, and X. J. Kang, Appl. Phys. Lett., 84, 2757 (2004)
- C.-F. Chu, F.-I. Lai, J.-T. Chu, C.-C. Yu, C.-F. Lin, H.-C. Kuo, and S. C. Wang, J. Appl. Phys., 95, 3916 (2004).
- J.-S. Ha, S. W. Lee, H.-J. Lee, H.-J. Lee, S. H. Lee, H. Goto, T. Kato, K. Fujii, M. W. Cho, and T. Yao, IEEE Photonics Technol. Lett., 20, 175 (2008)
- D.-S. Wuu, S.-C. Hsu, S.-H. Huang, C.-C. Wu, C.-E. Lee, and R.-H. Horng, Jpn. J.
- Appl. Phys., Part 1, 43, 5239 (2004).
  K.-M. Uang, S.-J. Wang, S.-L. Chen, Y.-C. Yang, T.-M. Chen, and B.-W. Liou, Jpn. J. Appl. Phys., Part 1, 45, 3436 (2006).
- S. J. Kim, J.-H. Jang, J.-S. Lee, and D. J. Duquette, Electrochim. Acta, 52, 5258
- S.-H. Huang, R.-H. Horng, S.-C. Hsu, T.-Y. Chen, and D.-S. Wuu, *Jpn. J. Appl. Phys., Part 1*, 44, 3028 (2005).
  S. J. Wang, K. M. Uang, S. L. Chen, Y. C. Yang, S. C. Chang, T. M. Chen, and C.
- H. Chen, Appl. Phys. Lett., 87, 011111 (2005).
- S. Y. Lee, K. K. Choi, H.-H. Jeong, H. S. Choi, T.-H. Oh, J. O. Song, and T.-Y.
- Seong, Semicond. Sci. Technol., 24, 092001 (2009).
  C. Huh, J. M. Lee, D. J. Kim, and S. J. Park, J. Appl. Phys., 92, 2248 (2002).
  C. Liu, Y. H. Chen, M. P. Houng, Y. H. Wang, Y. K. Su, W. B. Chen, and S. M. Chen, IEEE Photonics Technol. Lett., 16, 1444 (2004).
- H. Kim, K.-K. Kim, K.-K. Choi, H. Kim, J.-O. Song, J. Cho, K. H. Baik, C. Sone, Y. Park, and T.-Y. Seong, *Appl. Phys. Lett.*, **91**, 023510 (2007).
  I. V. Rozhansky and D. A. Zakheim, *Phys. Status Solidi C*, **3**, 2160 (2006).
  Y. C. Shen, G. O. Mueller, S. Watanabe, N. F. Gardner, A. Munkholm, and M. R.
- Krames, Appl. Phys. Lett., 91, 141101 (2007).
- A. A. Efremov, N. I. Bochkareva, R. I. Gorbunov, D. A. Larinovich, Yu. T. Rebane, D. V. Tarkhin, and Yu. G. Shreter, Semiconductors, 40, 605 (2006).
- 18. A. Hori, D. Yasunaga, A. Satake, and K. Fujiwara, Appl. Phys. Lett., 79, 3723 (2001).
- A. Y. Kim, W. Götz, D. A. Steigerwald, J. J. Wierer, N. F. Gardner, J. Sun, S. A. Stockman, P. S. Martin, M. R. Krames, R. S. Kern, et al., Phys. Status Solidi A, 188, 15 (2001).
- 20. B. Monemar and B. E. Sernelius, Appl. Phys. Lett., 91, 181103 (2007).
- S. F. Chichibu, T. Azuhata, M. Sugiyama, T. Kitamura, Y. Ishida, H. Okumura, H. Nakanishi, T. Sota, and T. Mukai, *J. Vac. Sci. Technol. B*, **19**, 2177 (2001).
- M. H. Kim, M. F. Schubert, Q. Dai, J. K. Kim, E. F. Schubert, J. Piprek, and Y. Park, Appl. Phys. Lett., 91, 183507 (2007).