NEAR-INTRINSIC MICROCRYSTALLINE SILICON FOR USE IN THIN FILM TRANSISTORS

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ABSTRACT

Inverted-staggered thin film transistors (TFTs) incorporating hydrogenated microcrystalline silicon for both contact and channel regions have been fabricated by plasma enhanced chemical vapour deposition (PECVD) using the high hydrogen-dilution method. The deposition parameters for the channel region were chosen to yield near-intrinsic material with a dark conductivity activation energy of 0.7 eV and a Tauc gap of 1.98 eV, while the doped contact layer was optimised to produce a high dark conductivity of 10 S/cm.

These devices exhibit a low off-current but the field effect mobility is found to be lower than that of similar devices incorporating an optimised amorphous silicon channel region. The mobility activation energy in these devices is similar to those incorporating an amorphous channel, but the mobility pre-factor is reduced. We propose that this is due to inhomogeneous conduction through a microcrystalline region with a smaller grain size at the dielectric/channel interface.

INTRODUCTION

Hydrogenated microcrystalline silicon (μc-Si:H) has recently shown promise as a material for microelectronics applications such as solar cells [1] and thin film transistors (TFTs) [2]. Consisting of variable size crystallites embedded within an amorphous matrix, it is expected to exhibit properties intermediate between those of hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si), hopefully retaining the large area and low temperature substrate compatibility of the former while improving the doping efficiency, conductivity and carrier mobility [3]. μc-Si:H is typically deposited by plasma enhanced chemical vapour deposition (PECVD) using silane highly diluted in hydrogen as source gases [4]. Refinements to this technique include the use of higher frequency power supplies than standard the 13.56 MHz [5], and the layer-by-layer technique [6],[7] whereby layers of a-Si:H are alternately deposited and then etched in a hydrogen plasma to remove the more disordered material. μc-Si:H typically exhibits a large optical band-gap [8], a low activation energy and high conductivity. A higher doping efficiency than a-Si:H allows for the production of highly conductive n-type films which are suitable for use as contact layers in TFTs and other devices [9].

Construction of entirely microcrystalline TFTs has, however, been hindered by the n-type character of the material which renders the channel highly conductive even in the off state. The precise reason for this characteristic is still unclear, though it has been proposed that oxygen contamination of μc-Si:H may result in the creation of donor-like defects, raising the Fermi level towards the conduction band edge [10]. Purification of source gases to remove oxygen contamination [10], or the use of light boron doping [2] can produce μc-Si:H where the Fermi level is near mid-gap, at the expense of an increase in the complexity of the deposition system.

In this work we investigate the performance of TFTs fabricated with a channel region that is inherently "near-intrinsic", that is the band-gap and activation energy are chosen to yield a

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Fermi level that is near mid-gap. This material is deposited solely using the high hydrogen-dilution method with neither source gas purification nor light boron doping. These TFTs utilise a bottom gate structure that is compatible with existing a-Si:H technology, in contrast with poly-Si TFTs which typically incorporate a top gate design [11]. The behaviour of these devices is contrasted with ones incorporating a low activation energy μc-Si:H channel region and devices that use an optimised a-Si:H channel. In all cases a highly conductive n+ μc-Si:H contact layer is used between the channel and source/drain metalisation.

EXPERIMENT

Deposition of μc-Si:H

The μc-Si:H for the TFT channel and contact layers was deposited using a commercial, capacitively coupled 13.56 MHz PECVD system (Plasma Technology DP80). Electrode separation was 40mm and diameter 255mm. Prior to TFT fabrication, potential films for the channel region were characterised over a range of deposition powers. Other deposition conditions were kept constant, as indicated in Table I. Deposition times were adjusted to yield films of approximately 3000 Å thickness in all cases. Films were deposited on Corning 7059 glass for optical and conductivity measurements, and low-doped (10 Ωcm) p-type silicon wafers for infra-red transmission and X ray diffraction measurements.

Table I. Deposition Conditions for Possible Channel Layers

SiH_4	H_2	Temperature	Pressure	Power
9 sccm	450 sccm	250 °C	400 mTorr	25 W - 250 W

Activation energy and conductivity for these films are shown in Figure 1 and Figure 2.

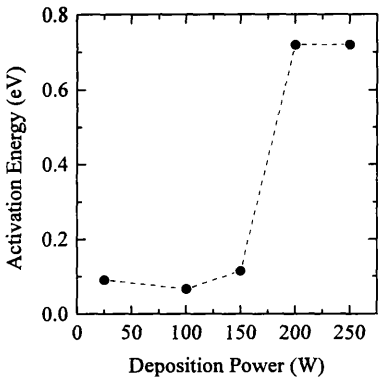

Figure 1. Activation Energy vs. Deposition Power

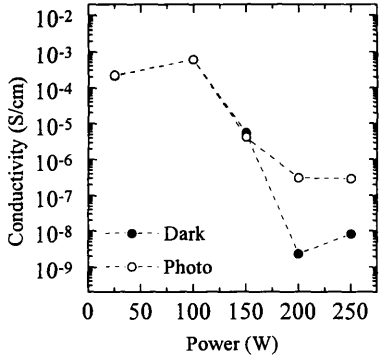

Figure 2. Dark and Photo-conductivity (AM1) vs. Deposition Power

The sharp increase in activation energy with increasing deposition power suggests that μc-Si:H

with Fermi Level near mid-gap may be produced using only high hydrogen dilution, based on a Tauc gap of 1.9 eV determined from the UV/visible spectroscopy data.

The increase in the ratio of photo to dark conductivity shown in Figure 3 is indicative of a decrease in the density of defects in the μc-Si:H band gap. This decrease in defect density may be attributed either to an increase in hydrogen passivation of dangling bonds with increasing power, or by the enhanced etching of more disordered material [12]. Furthermore, the X ray diffraction data for these films (Figure 4) shows an increase in the intensity of the silicon <111> peak with increasing deposition power, indicating a transition from amorphous to crystalline material. Using the Scherrer formula a crystallite size of 55 Å is predicted for films deposited at 250 W. As the deposition power is increased the intensity of the <111> peak at $2\theta = 28°$ is reduced, suggesting the onset of over-etching.

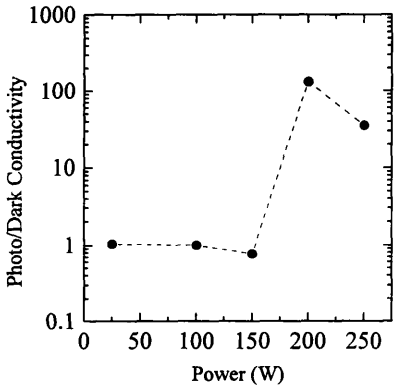

Figure 3. Ratio of Photo to Dark Conductivity vs. Deposition Power

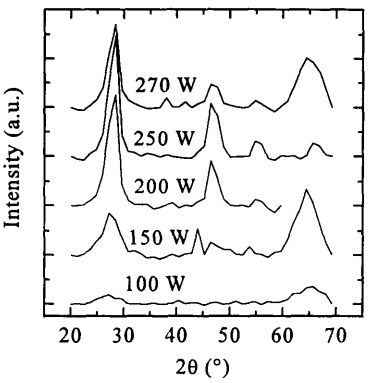

Figure 4. X Ray Diffraction Spectra for Varying Deposition Powers

Fabrication of TFTs

TFTs were manufactured to an inverted-staggered design with a highly doped n+ silicon wafer (0.02 Ωcm) forming a common gate electrode. 4000 Å of PECVD SiO_2 was used as a gate dielectric as this material has been used previously to produce test transistors [13] and readily provides a comparison between different channel materials. The formation of the dielectric was immediately followed by the deposition of 3000 Å of material to form the channel region. Material from both the low (100 W) and high (250 W) activation energy regions of Figure 1 has been used for the channel region. In addition reference TFTs were manufactured using 3000 Å of optimised a-Si:H for the channel. Finally 500 Å of n+ μc-Si:H was deposited on top of the channel region as a contact layer. This material has a conductivity of approximately 10 S/cm, and was deposited using conditions based on work presented in [9]. The deposition conditions for all channel regions and the contact layer are shown in Table II.

Table II Deposition Conditions for TFT Layers

Material	SiH_4	H_2	1% PH_3 in H_2	Temperature	Pressure	Power	Time
a-Si:H	80 sccm			300 °C	300 mTorr	10 W	16 min
μc-Si:H (1)	9 sccm	250 sccm		250 °C	400 mTorr	100 W	75 min
μc-Si:H (2)	9 sccm	450 sccm		250 °C	400 mTorr	250 W	40 min
n+ μc-Si:H	5 sccm	450 sccm	7.5 sccm	200 °C	500 mTorr	54 W	25 min

Source/drain metalisation was thermally evaporated aluminium, with a initial layer of chromium to prevent thermal diffusion of the aluminium into the contact layer. Source and drain regions were defined with a wet chemical etch of the metalisation and n+ contact layer, while individual devices were isolated using a CF_4 plasma etch.

RESULTS

The mask set used for the patterning of the TFTs describes devices of several different geometries. For the following measurements structures with W/L ratios of 40.4 and 11.7 were used; transfer characteristics have been normalised to a W/L ratio of 1 in all cases. TFT parameters were extracted from gate transfer characteristics conducted over the range V_{gs} = -25 to 75 V at V_{ds} = 1 V. Mobility and threshold voltage were calculated in the linear region by a least-squares fit to the gate transfer data, while the pre-threshold slope was calculated via a least-squares fit in the sub-threshold region. Gate transfer characteristics for the three types of channel regions are shown in Figure 5. A summary of the parameters extracted from the typical TFTs in each batch may be found in Table III.

Table III. TFT Characteristics by Channel Region

Device	Channel Region	Mobility	Threshold Voltage	Pre-threshold Slope	On/Off Ratio
1	μc-Si:H (100W)	0.14 cm^2/Vs	49 V	0.06 decades/V	10^3
2	μc-Si:H (250W)	0.15 cm^2/Vs	43 V	0.16 decades/V	10^5
Reference	a-Si:H	0.59 cm^2/Vs	43 V	0.18 decades/V	10^6

The high threshold voltage is due to the use of a thick layer of PECVD oxide as the gate dielectric, resulting in slow turn-on of the devices. Properties of this dielectric have previously been discussed in [14]. The output characteristics of both a-Si:H and μc-Si:H devices show no evidence of current crowding; hence it is assumed that the Cr/Al metalisation provides a good ohmic contact to the n+ contact layer, and that the n+ layer provides sufficient carrier injection into the channel region.

As expected from the conductivity data shown in Figure 2 the channel region of the Type 1 devices exhibits the lowest On/Off ratio and the lowest pre-threshold slope. This corresponds to the Fermi Level being swept through a high defect density as the device is turned on [13]. Type 2 also show significantly inferior characteristics relative to the reference devices. Variation of gate transfer characteristic with temperature for Type 2 devices is shown in Figure 6, while the temperature dependence of mobility is thermally activated (Figure 7) and given by:

$$\mu = \mu_0 \exp\left(-\frac{E_a}{kT}\right) \quad (1)$$

It is clear that the difference in mobility between Type 2 and reference devices is due to differing values of the mobility pre-factor, μ_0, and that the activation energy is similar between both sets of devices. The low pre-factor suggests a lower density of accessible states for the extended state conduction, which is consistent with inhomogeneous conduction in the microcrystalline layer. Furthermore the low value of the mobility activation energy suggests a grain size smaller than the 50 Å found by X ray diffraction. The hypotheses of low grain size and inhomogeneity during the initial stages of deposition are respectively supported by TEM [15] and spectroscopic ellipsometry [16].

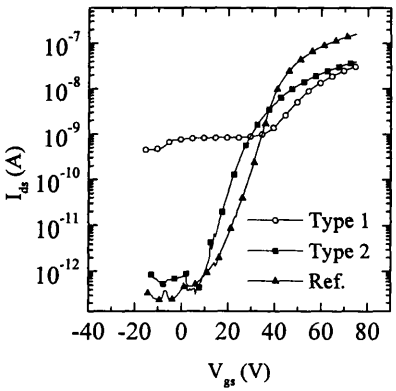

Figure 5. Sub-threshold Region

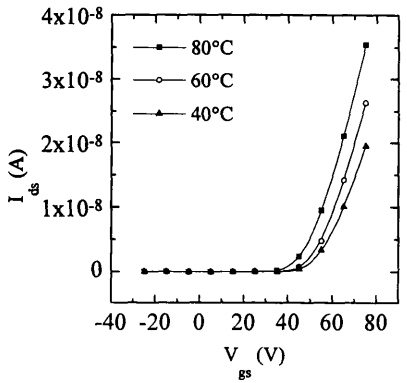

Figure 6. Temperature Dependence of Linear Region for Type 2 Devices

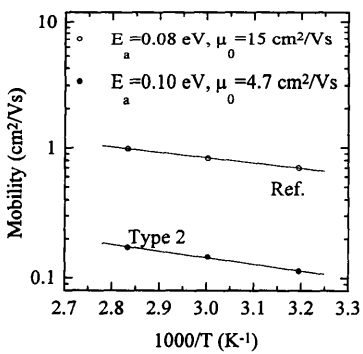

Figure 7. Temperature Dependence of Mobility

CONCLUSIONS

Near-intrinsic microcrystalline silicon has been deposited by PECVD without the use of source gas purification or light boron doping. A critical power (~150 W) is observed below

which films deposited by this method exhibit high conductivity, low activation energy, and little crystallinity. Above this power increased activation energy, reduced conductivity and increased crystallinity are observed; such films have a Fermi Level that is near mid-gap. Bottom gate devices fabricated using this material as a channel region are compatible with existing a-Si:H technology and exhibit an off-current sufficiently low for device applications; field effect mobility remains, however, lower than conventional a-Si:H channel devices. Based on the observation that this is predominantly due to differences in the mobility pre-factor we propose that conduction in these devices occurs inhomogeneously through a region of fine-grained material formed during the initial stages of channel deposition. Further research is required to determine whether the quality of this interfacial region may be improved while still retaining the existing device structure.

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REFERENCES

1. K. Saitoh, N. Ishiguro, N. Yanagawa, H. Tanaka, M. Sadamoto, S. Fukuda, Y. Ashida and N. Fukuda, J. Non-Cryst. Solids, **198-200**, 1093-1096, (1996)
2. S. S. He and G. Lucovsky, Mat. Res. Soc. Symp. Proc., **336**, 25-30, (1994)
3. A. Mireshghi, W. S. Hong, J. Drewery, T. Jing, S. N. Kaplan, H. K. Lee and V. Perez-Mendez, Mater. Res. Soc. Proc. Spring, (1994)
4. A. Matsuda, J. Non-Cryst. Solids, **59 & 60**, 767-774, (1983)
5. F. Finger, P. Hapke, M.Luysberg, R. Carius, H. Wagner and M. Scheib, Appl. Phys. Lett, **65**, 20, 2588-2590, (1994)
6. M. Fang, J. B. Chevrier and B. Drévillon, J. Non-Cryst. Solids, **137 & 138**, 791-794, (1991)
7. K. C. Park, S. K. Kim, M. Park, J. M. Jun, K. H. Lee and J. Jang, Solar Energy Materials, **34**, 509-515, (1995)
8. D. G. Moon, B. H. Jung, J. N. Lee, B. A. Ahn, H. B. Im, K. S. Nam and S. W. Kang, **5**, 364-369, (1994)
9. S. C. Saha and Swati Ray, J. Appl. Phys., **78**, 9, 5713-5720, (1995)
10. P. Torres, J. Meier, R. Flückiger, U. Kroll, J. A. Anna Selvan, H. Keppner, A. Shah, S. D. Littlewood, I. E. Kelly and P. Giannoulès, Appl. Phys. Lett, **69**, 10, 1373-1375, (1996)
11. H. J. Lim, B. Y. Ryu and J. Jang, Appl. Phys. Lett, **66**, 21, 2888-2890, (1995)
12. R. C. van Oort, M. J. Geerts, J. C. van den Heuvel and J. W. Metselaar, Electronics Letters, **23**, 18, 967-968, (1987)
13. F. J. Clough, Cambridge University Ph.D. Thesis, (1991)
14. S. C. Deane, F. J. Clough, W. I. Milne and M. J. Powell, J. Appl. Phys., **73**, 6, 2895-2901, (1993)
15. L. C. Wang, D. Feng, T. Epicier, C. Esnouf, H. Xia, Y. L. He, Q. Li, Y. M. Chu and N. B. Ming, Appl. Phys. Lett, **66**, 8, 968-970, (1995)
16. Y. H. Yang, M. Katiyar, G. F. Feng, N. Maley and J. R. Abelson, Appl. Phys. Lett, **65**, 14, 1769-1771, (1994)