A 960-fps Sub-sampling Object Extraction CMOS Image Sensor with 12-bit Column Parallel ADCs and ALUs

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ABSTRACT

A CMOS image sensor with highly accurate object extraction pre-processing functions by 960-fps sub-sampling operation, 12-bit column parallel successive approximation ADCs and column parallel ALUs has been developed. The pixel is composed of four transistors type pixel which shares the source follower transistor and the pixel select transistor. The each ADC is composed of the noise and signal holding capacitance, the noise reduction circuit, the comparator and the small DAC that combined both the reference voltage ratios and capacitance ratios. In the ALU, the object categorization pre-processing is performed by the each macro block of 3 x 3 pixels which has a reference pixel and its neighboring eight pixels. The three image features which are the edge of object, the direction of edge-vector and the average of light-intensity of 3 x 3 pixels corresponded to each pixel are extracted by the ALUs. The image and the results of the object extraction pre-processing are outputted by every 60-fps. The image sensor was fabricated by 0.35-μm 2P3M technology. The pixel pitch is 5.3-μm, the number of pixels is 640H x 360V and the chip size is 4.9-mm square.

Keywords: Image sensor, column parallel A/D converter, object extraction, real time image processing

1. INTRODUCTION

A technology of object categorization is highly demanded in various applications, such as, human recognition, scene segmentation, monitoring FA/ITS and image database construction.

The several recent papers have reported the solution to realize the real time high-functional image processing. One of the conventional approaches is that the image processing is performed to an image data, which outputted from a high quality image sensor, by hardware or software. In this approach, very high-speed processor is required to achieve real time image processing because of limiting to performance of the processor. The other approach is that the image sensor, which has a processor in pixel such as vision chip, performs high-functional and high-speed operation. In this approach, it is difficult to increase the number of pixels because of the large pixel equipped with processor.

In order to solve abovementioned issue, the high-functional CMOS image sensors equipped with column parallel processors have been reported [2-4]. Those image sensors have the capability of outputting high quality image data and image features for reducing the cost of high-functional image processing operation at the same time. However, the size of pixel, A/D Converter (ADC) and Arithmetic Logic Unit (ALU) is too large to increase the number of pixels. The resolution of the ADC is 8-bit and it is low. The operating frequency of the ALU is too high for the number of pixels.

In this paper, the ADC and the ALU are modified of the number of pixel, the resolution of the ADC, the operating speed and the function of the image processing. The CMOS image sensor with high quality image and preprocessing function of highly accurate object extraction by 960-fps sub-sampling 12-bit column parallel ADCs and ALUs is reported.

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2. IMAGE SENSOR DEVICE AND A/D CONVERTER

Fig.1 shows the chip photograph of the image sensor and the block diagram. The image sensor is composed of the sensor pixel array, the analog memory, the column parallel ADCs, the SRAM, the column parallel ALUs and those drivers.

Fig.2 shows the schematic diagram and the timing chart of the pixel, the analog memory and the column parallel ADCs. The pixel circuit is four transistors type sharing source follower and pixel select transistor by two pixels. The size of pixel is 5.3-μm square and fill factor is 18%. The reduction of the noise caused by for threshold voltage variations of MOS transistor and thermal reset noise at pixel floating diffusion node is achieved by the combination of the sample-hold and the A/D conversion operation.

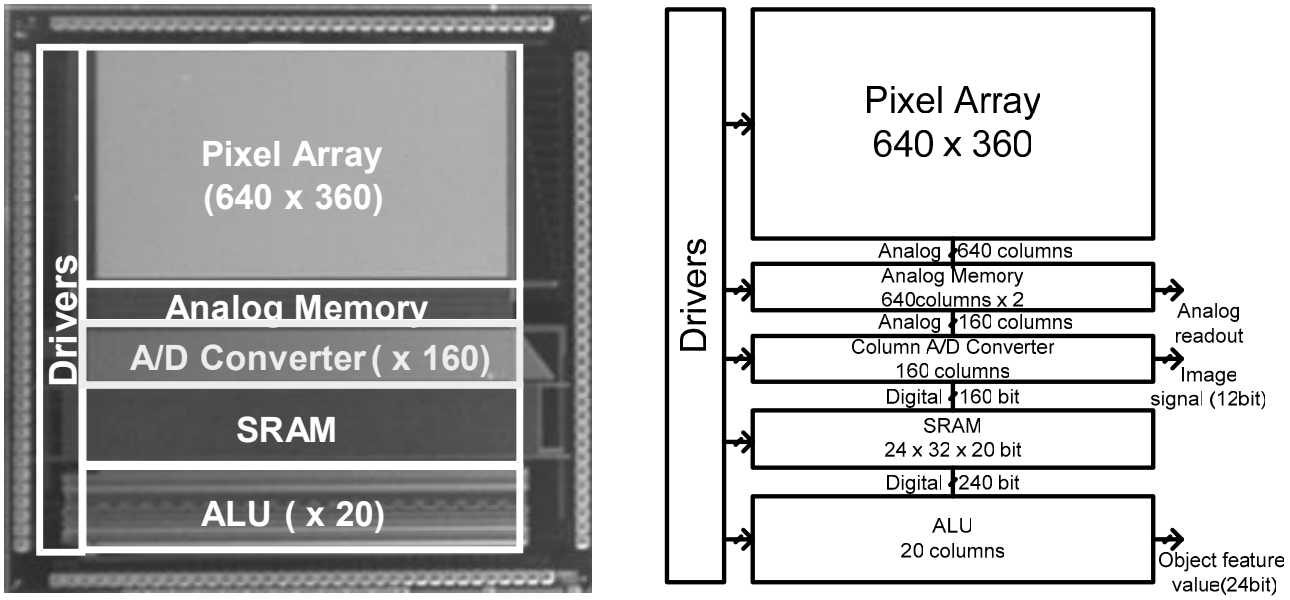


Fig.1 The chip photograph and the block diagram.

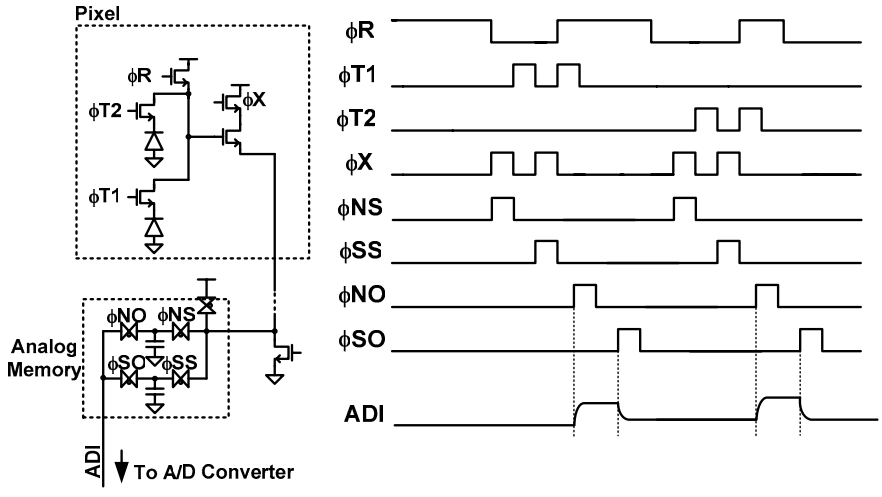


Fig.2 The schematic diagram and the timing chart of pixel and analog memory.

Fig.3 shows the schematic diagram and the timing chart of the successive approximation ADC (SAADC). The SAADC is composed of the comparator and the reference voltage supply circuit, and it is shared by 4-column pixels.

The SAADC is able to perform A/D conversion operation without high-frequency driving signal because the numbers of A/D conversion steps are the number of bits. And it is suitable for integrating on the sensor chip because of achieving the noise reduction and the A/D conversion at the same time.

The conventional SAADC has binary-weighted reference voltages generated by one reference voltage and some binary-weighted capacitors and is too large to integrate on the sensor chip, because the binary-weighted capacitor array is too large. In order to improve the issue of the area, the SAADC whose binary-weighted reference voltages are generated by two reference voltages and the binary-weighted capacitor array has been reported [5].

However, the smaller ADC is required to achieve increasing the number of pixels and the resolutions, and the on-chip high-functional operation.

In this paper, the SAADC whose binary-weighted reference voltages are generated by twelve reference voltages and two binary-weighted capacitors is developed. The SAADC is achieved reducing the number of the binary-weighted capacitors, and the number of capacitors of that SAADC is two hundred times as little as the number of capacitors of the conventional SAADC. The reference voltage that supplies to the SAADC is able to tune its gain and linearity of A/D conversion by the control from the outside.

The fabricated SAADC has 12-bit of the resolution, 200μV of the LSB and 1.84MC/sec of the conversion rate that corresponds to 300MC/sec for serial readout. The 12-bit digital signal is outputted as an image signal, and the object categorization pre-processing is performed to the higher-order 4-bit digital signal stored in the SRAM.

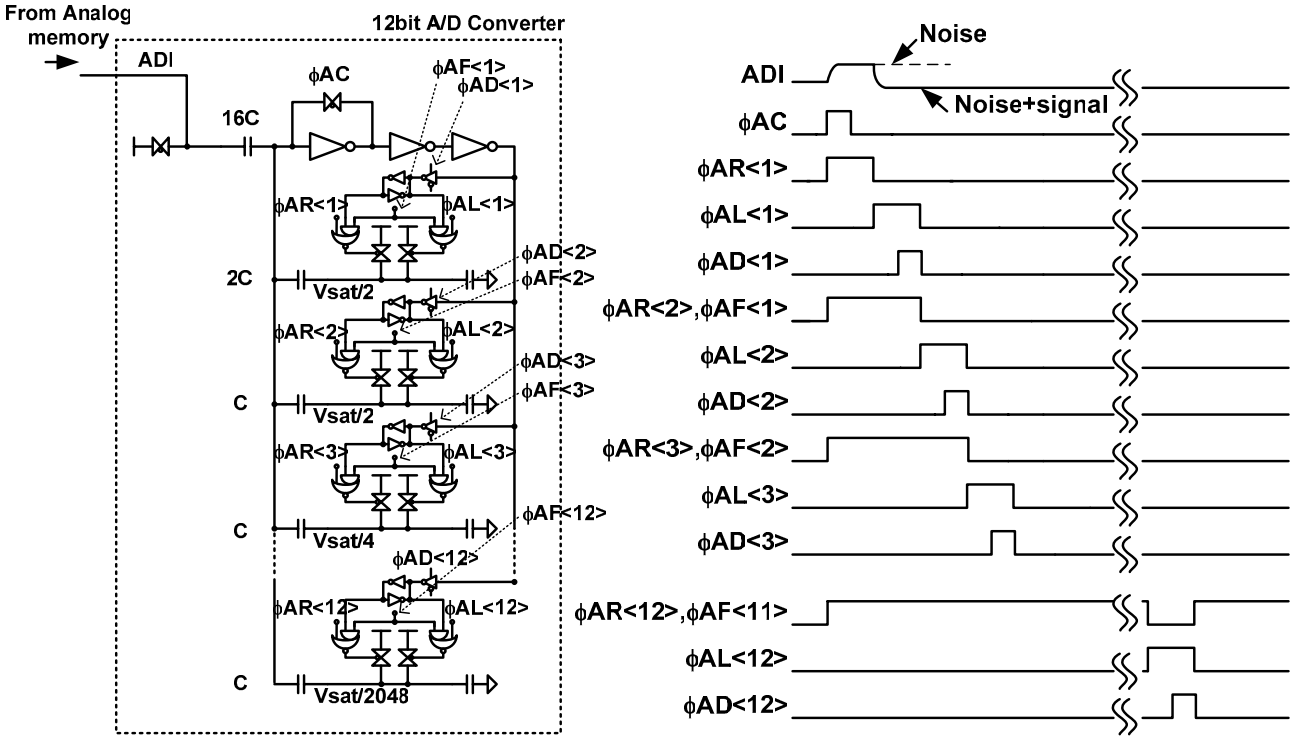
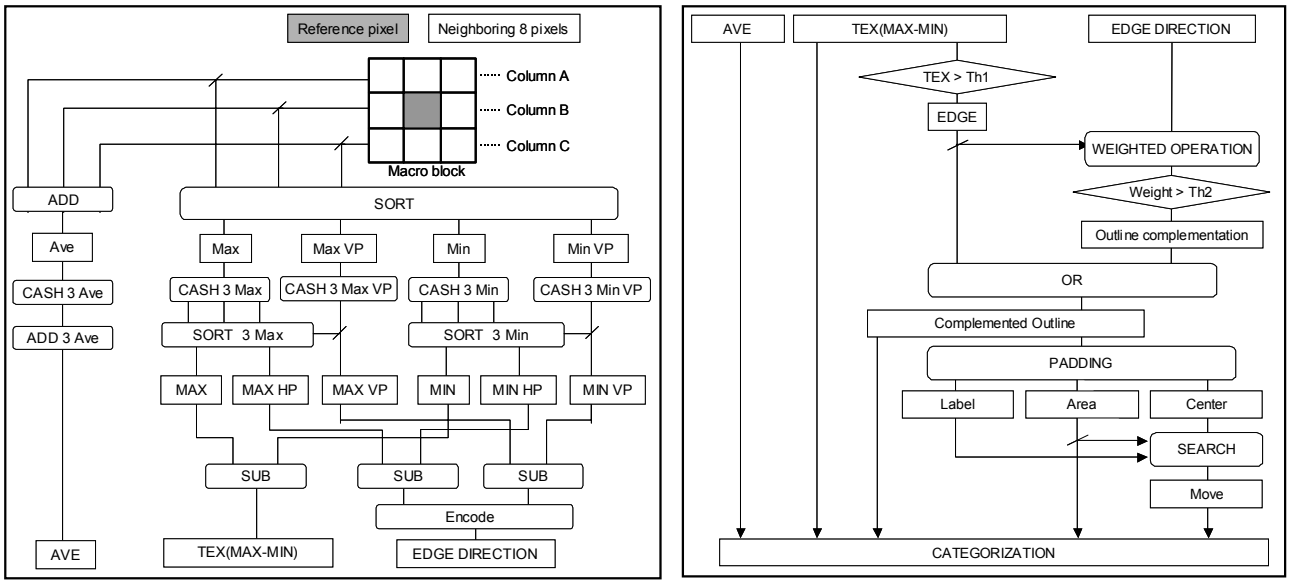


Fig.3 The schematic diagram and the timing chart of ADC.



(a) The flow chart of the object extraction algorithm; on-chip (b) The flow chart of the object categorization algorithm; off-chip

Fig.4 The object categorization algorithm flow chart.

3. OBJECT EXTRACTION FOR THE OBJECT CATEGORIZATION PRE-PROCESSING

Fig.4 (a) and (b) show the flow chart of the object categorization pre-processing algorithm which operated at on-chip ALU and off-chip.

The object categorization is achieved by operating the image features of the connected-component and the segmented-image that is calculated by operating the image features of the outline-component. The connected-component and the outline-component are calculated by operating the image features of the low-frequency and the high-frequency. The object categorization pre-processing, which is suitable for the parallel-processing and is achieved by small processor, is required for integrating on the sensor chip. The on-chip ALU has a low-frequency component and a high-frequency component. The area segmentation and the object categorization are performed outside of the sensor chip.

The image sensor operates the image features extraction operation to all pixels every the each macro block (MB) of 3x3 pixels which is composed a reference pixel and 8 neighboring pixels. The small processor that is achieved by operating to the MB is able to integrate many processors in parallel on the image sensor chip. And, it operates many operations in real time without high-speed processor that consumes much power consumption.

The ALU operates three image features extraction as follows; At first, the edge is extracted by operating the image feature of the high-frequency defined the texture in order to segment the objects. The edge binary data of the object are calculated by extracted texture data. And the outline data composed by the edge data generate the area segmentation data. Next, the direction of edge-vector by which can be speculated the local outline is extracted in order to complement outline defect resulting from the noise influence and the overlap of objects. Finally, the average of light-intensity that is used at the object categorizing operation at the off-chip is extracted to the 9 pixels in the MB.

First of all, the texture what is the difference between the maximum light-intensity value (MAX) and the minimum light-intensity value (MIN) in the MB, is operated (TEX=MAX-MIN), and it is outputted with 4-bit digital code. Moreover, this operation achieves high-speed and the reduction of the area by the pipeline operation.

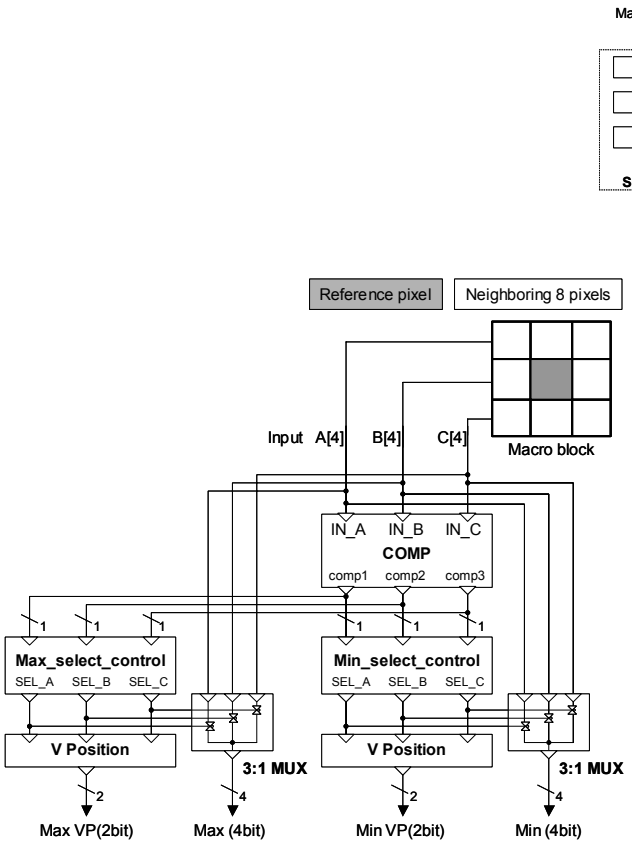
The comparison operation to calculate the MAX and the MIN in the MB is achieved of the following two steps. In the first step, the maximum light-intensity value (Max) and the minimum light-intensity value (Min) of each row in the MB are operated. In the second step, the MAX value is operated from among three Max values that are operated each row,

similarly the MIN value is operated from among three Min values that are operated each row. Simultaneously, the position data of the MAX value and the MIN value in the MB is outputted. The position data are 4-bit digital code that consists of 2-bit digital code of the horizontal position (HP) and the vertical position (VP) in the MB.

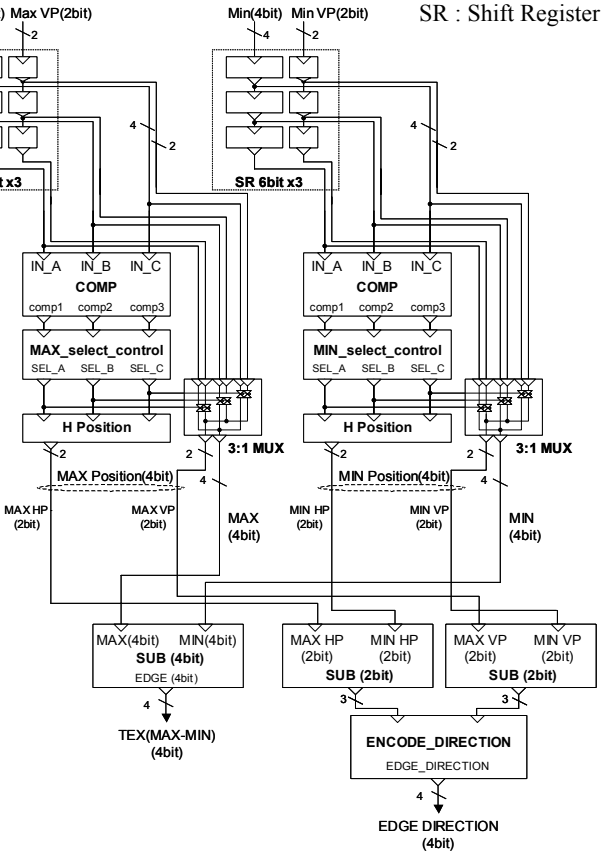
Next, the direction of edge-vector (EDGE DIRECTION) that is the normal direction of the position of the MIN (MIN Position) to the position of the MAX (MAX Position) is categorized to 16 directions, and outputted with 4-bit digital code. The direction of edge-vector is calculated from encoded value of difference between the MAX Position value and the MIN Position value for each horizontal and vertical position data. The noise tolerance and the performance of completing a closed curve of outline-component are improved by complementing outline defect at the off-chip using this result. Fig.5 shows (a) first step comparison and sort operation circuit, (b) second step comparison, sort operation circuit, edge extraction circuit and direction of edge-vector encode circuit.

And, the average of light-intensity (AVE) of 9 pixels in the MB is operated 4-bit digital code. This is used as a kind of image features in the object categorizing operation. Fig.6 shows the block diagram of the AVE value extraction circuit.

At the off-chip, the operations to the object categorization are performed by using the image features that are extracted at the on-chip. First of all, threshold judgment to extract the edge data is operated for the texture extraction result. Here, the threshold value (Th1) can be set flexibly at the off-chip. Moreover, the outline complementation is operated by following operations. The weighted operation is operated for each pixel along the direction of edge-vector, and the



(a) First step comparison and sort operation circuit



(b) Second step comparison, sort operation circuit, edge extraction circuit and direction of edge-vector encode circuit

Fig.5 Block diagrams of on-chip ALU.

Threshold judgment (Th2) is operated for each pixel every time weighted operation of one line is completed. As mentioned above, a highly accurate closed curve can be extracted by combining the edge extraction result and the outline complement operation, as a result, highly accurate area segmentation can be performed. And, the object categorization is well performed by judging the image features in the area.

4. EXPERIMENT RESULT AND DISCUSSION

Table.1 shows the specifications and performances of this trial image sensor. This image sensor was produced experimentally in 0.35-μm 2P3M technology. Pixel pitch is 5.3-μm, and the number of pixels is 640H x 360V and the die size is 4.9-mm square.

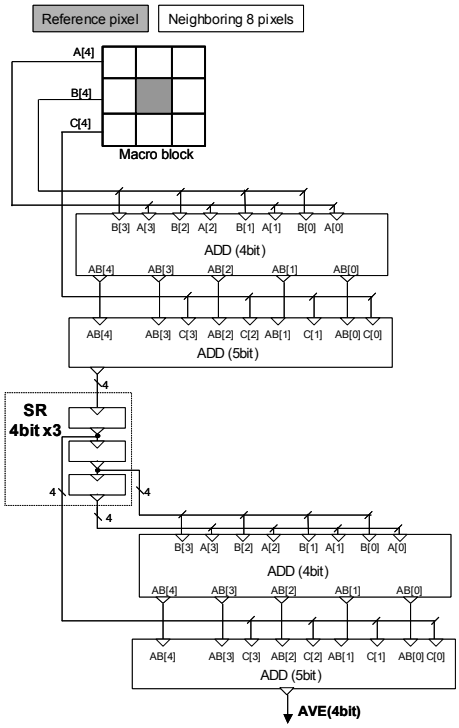
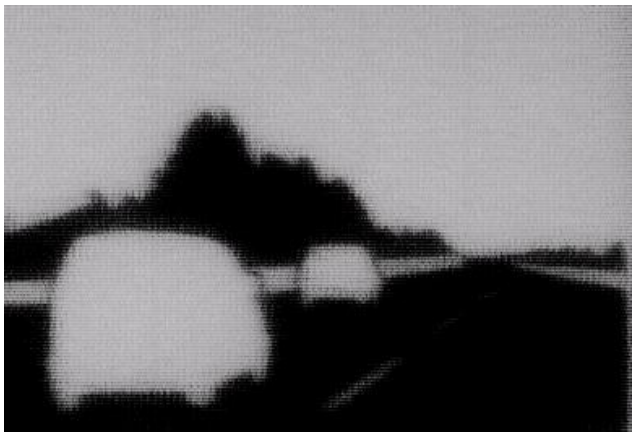


Fig.6 Average operation circuit.

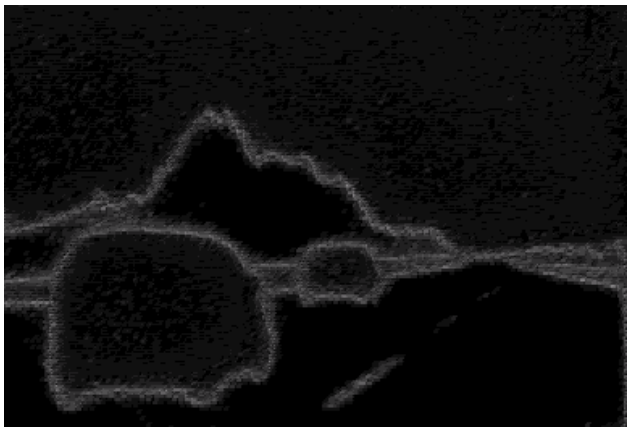
Table.1 Specifications and performances

Technology	0.35μm 2P3M CMOS
Power supply	3.3[V]
Die size	4.9mm x 4.9mm
Number of the pixel	640 x 360 pixels
Number of the A/D converter	160
Resolution(sub-frame data)	12[bit]
Size of the pixel	5.3μm x 5.3μm
Size of the photodiode	2.25μm x 2.25μm
Fill factor	18[%]
Effective conversion rate	1.84[MS/sec]
Maximum signal amplitude	819.2[mV]
Minimum input voltage	200[μV]
Image feature extraction of ALU	AVERAGE 4[bit], TEXTURE 4[bit], EDGE DIRECTION 4[bit]
Operation frequency of ALU	22[MHz]

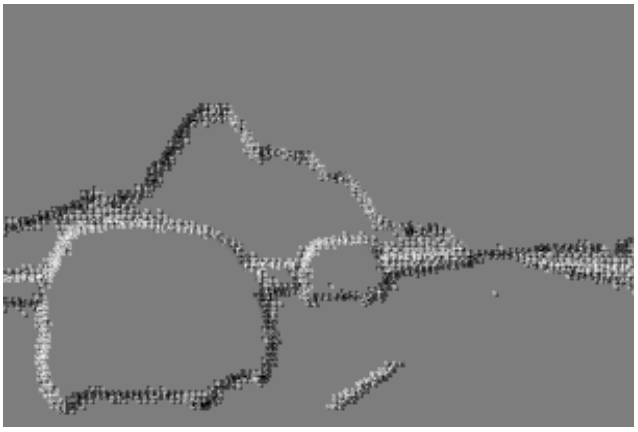


(a) Original image

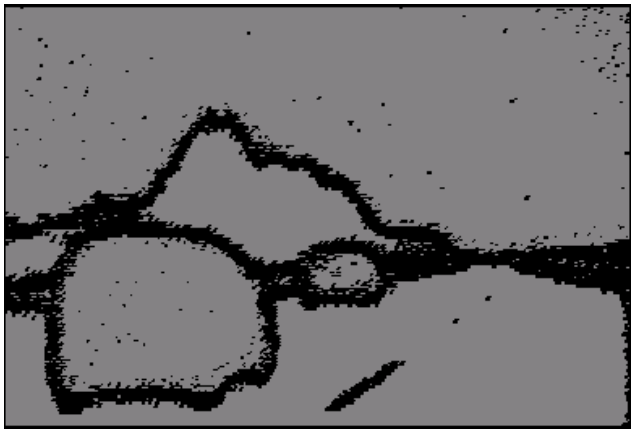
(b) The result of AVE extraction



(c) The result of TEX extraction



(d) The result of EDGE DIRECTION extraction



(e) The result of outline complementation ((c)+(d))

(f) The result of area segmentation

Fig.8 Experimental result image.

Fig.8 shows (a) original image, (b) the result of AVE extraction, (c) the result of TEX extraction, (d) the result of EDGE DIRECTION extraction, (e) the result of outline complementation ((c)+(d)) and (f) the result of area segmentation. Fig.8 (a) shows the image that is taken picture to have schematically illustrated car and road. Fig.8 (d) shows EDGE DIRECTION as the gray-scale image corresponded to 16 edge directions. Fig.8 (e) shows the image that outline is complemented and made to binary using the edge extraction result and the direction of edge-vector extraction result. Fig.8 (f) shows the result of area segmentation data calculated by PADDING processing using the result of (e).

As a result, it is found that the area segmentation is well performed by using the edge extraction result that is operated TEX and the outline complementation with EDGE DIRECTION.

5. CONCLUSION

The CMOS image sensor having the capabilities of the 12-bit A/D converter, the object categorizing pre-processing at every 960-fps image and the high quality image signal output is developed.

The image sensor is designed and produced experimentally with object categorizing pre-processor. Object categorizing pre-processor calculates the average which is used at the object categorizing operation as a kind of image features, the extraction of texture is operated to calculate the edge that is important as area segmentation of each object and the direction of edge-vector for improving the noise tolerance and the performance of completing a closed curve are operated. The above-mentioned image features at every 960-fps image were outputted from the image sensor, and the number of the area segmentation processing in the off-chip can be reduced. As a result, the high-speed real time object extraction system is developed. The image sensor can be utilized in various image-processing applications.

REFERENCES

1. T. Komuro, I. Ishii, M. Ishikawa, A. Yoshida, “A Digital Vision Chip Specialized for High-Speed Target Tracking” IEEE Transaction on Electron Devices, 50(1), 191-199 (2003).
2. S. Sugawa, T. Tate, K. Chiba, K. Kotani and T. Ohmi, “A High S/N Ratio CMOS Image Sensor with Real Time Object Categorizing Function” IEEE Workshop on CCD&AIS, 212-216 (2003).
3. T. Tate, S. Sugawa, K. Chiba, K. Kotani and T. Ohmi, “A High S/N Ratio Object Extraction CMOS Image Sensor with Column Parallel Signal Processing” Solid State Devices and Materials, 354-355 (2004).
4. T. Tate, S. Sugawa, K. Chiba, K. Kotani and T. Ohmi, “A High S/N Ratio Object Extraction CMOS Image Sensor with Column Parallel Signal Processing” Japanese Journal of Applied Physics, 44(4B), 2093-2098 (2005).
5. A. I. Krymski, N. E. Bock, N. Tu, D. Can Blerkom, E. R. Fossum, “A High-Speed, 240-Frames/s, 4.1Mpixel CMOS Sensor” IEEE Transaction on Electron Devices, 50(1), 130-135 (2003).