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# Structure, Chemistry, and Electrical Performance of Silicon Oxide-Nitride-Oxide Stacks on Silicon

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The structure and chemistry of silicon oxide-nitride-oxide (ONO) stacks on silicon with differently processed top oxide layers were analyzed using high-resolution transmission electron microscopy, electron energy loss spectroscopy, secondary ion mass spectroscopy, and X-ray specular reflectometry. The changes observed in the structure and chemistry of the ONO stacks were correlated with the electrical performance of these stacks in flash-memory devices. The results demonstrated that using larger thermal budgets to form the top oxide layer yields (*i*) broader N distribution across the nitride/oxide interfaces, (*ii*) reduced H content at the $Si/SiO_2$ interfaces, (*iii*) increased density of the top oxide layer, and ultimately, (*iv*) improved electrical performance of ONO-based memory devices.
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Silicon oxide-nitride-oxide amorphous multilayers (ONO stacks) attract considerable interest as the charge-storage media in nonvolatile memory devices.[1,2] Ultrathin ONO stacks are commonly prepared by thermal growth of a $SiO_2$ layer (bottom oxide) on silicon, followed by low-pressure chemical vapor deposition (LPCVD) of $Si_3N_4$. Subsequently, the top oxide is either grown by the nitride reoxidation or deposited by LPCVD. The typical thickness of individual layers in the ONO stacks ranges from 5 to 15 nm. The critical structural and compositional parameters that affect electrical performance of the ONO-based devices include the physical density of the amorphous oxide/nitride layers and the depth distributions of the oxygen, nitrogen, and hydrogen atoms. Few systematic studies that analyze the effect of processing conditions on these parameters in stacked ONO structures have been reported.[3-6] Some of these studies observed ONO stacks to consist of well-defined layers of $SiO_2$ and $Si_3N_4$[3,4] with no significant nitrogen content in the oxide layers. Other studies[5,6] revealed considerable concentration of nitrogen in the top oxide layer of the ONO stacks, as well as the segregation of nitrogen to the bottom $SiO_2/Si$ interface. Reports of artifacts associated with nitrogen segregation to the $SiO_2/Si$ interface during spectroscopic measurements[7,8] added to the confusion in the interpretation of the existing data. The optimal (from the electrical performance point of view) nitrogen profile in the bottom oxide of ONO stacks remains a subject of debate.[9,10] At present, incomplete understanding of the processing-structure/chemistry-properties relations impedes rational optimization of the processing parameters for the ONO stacks. The present work is aimed at a systematic study of these relations in the ONO stacks for flash-memory applications. We applied both spatially resolved electron energy loss spectroscopy (EELS) in a transmission electron microscope (TEM) and secondary ion mass spectroscopy (SIMS) to analyze elemental distributions in the differently processed ONO stacks, while the densities of individual layers in these stacks were determined using X-ray specular reflectometry (XRR). The results of structural/compositional analyses were subsequently correlated with the electrical performance of the ONO stacks in flash-memory devices.

## Experimental

The ONO stacks chosen for this study consisted of a thermally grown bottom oxide (6-7 nm), a silicon nitride (6-15 nm) layer deposited from the mixture of $SiCl_2H_2$ and $NH_3$ using LPCVD, and a top oxide (8-13 nm) formed either by nitride reoxidation (ONO-S, ONO-L) or deposited using LPCVD from tetraethoxysilane (TEOS) (ONO-TEOS); the processing conditions are summarized in Table I. The processing parameters were adjusted to obtain similar thicknesses of the corresponding layers in different ONO stacks.

The X-ray specular reflectometry measurements were conducted using automatic grazing incidence Rigaku[f] $CXR^2$ X-ray reflectometer equipped with a rotating anode generator and a channel-cut Ge (220) monochromator. Cu $K\alpha_1$ radiation was used. The incident and reflected beams were collimated and the reflected intensity was measured by a scintillation counter. The specular reflectivity was recorded in a $2\theta$ scan from 0 to 10°. The density and thickness of each layer in the stack, as well as the interfacial roughness, were determined by analysis of the experimental data using commercial Rigaku software.

The cross-sectional specimens for TEM were prepared by conventional sectioning, grinding, and polishing followed by dimpling to a thickness of 25 μm. The thinning was completed until perforation either in the Gatan precision ion-polishing system (5 kV, 4°) or in the South Bay ion-milling system (5 kV, 10°) with the specimen cooled to −80°C; both ion-thinning procedures produced similar results. Phase-contrast imaging and some EELS measurements were conducted in a JEOL-3010 UHR (300 kV, $LaB_6$ source) HRTEM equipped with a GATAN imaging filter (GIF). Recently, we reported

[f] The identification of any commercial product or trade name does not imply endorsement or recommendation by the National Institute of Standards and Technology.

**Table I. Processing of ONO structures.**

| Specimen | Processing |
|---|---|
| ONO-S | 1. Bottom oxide: dry oxidation in dilute $O_2$ at 900°C.<br>2. Silicon nitride: LPCVD in ($SiH_2Cl_2$ plus $NH_3$) mixture at 700°C.<br>3. Top oxide: steam oxidation at 1000°C. |
| ONO-L | Larger (×2) initial thickness of nitride layer<br>Longer nitride reoxidation |
| ONO-TEOS | TEOS top oxide (670°C) |
| ON | Stacked oxide-nitride structure |
| BOX | Single-layer thermal oxide |

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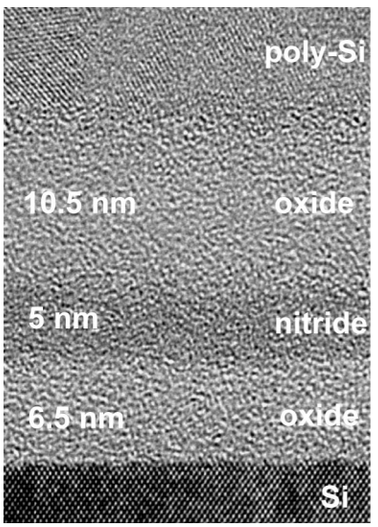


**Figure 1.** Typical HRTEM image of ONO stack. (The image was recorded from the ONO-TEOS specimen.)

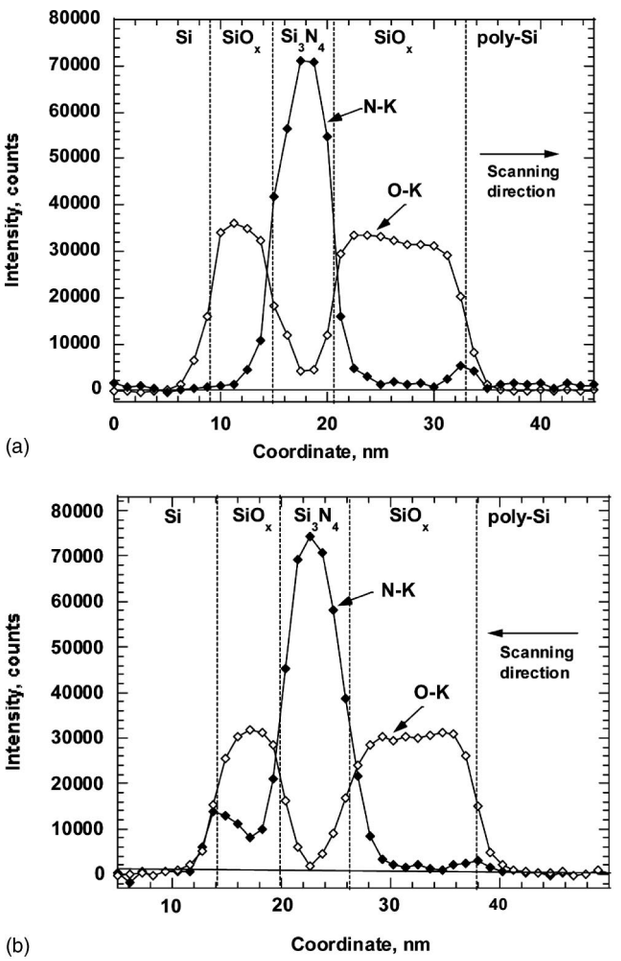


**Figure 2.** Profiles of the O-K and N-K integrated intensities across the ONO-L stack for the beam-scans which originated in the (a) Si-substrate and (b) poly-Si cap layer. Similar profiles were obtained for ONO-TEOS.

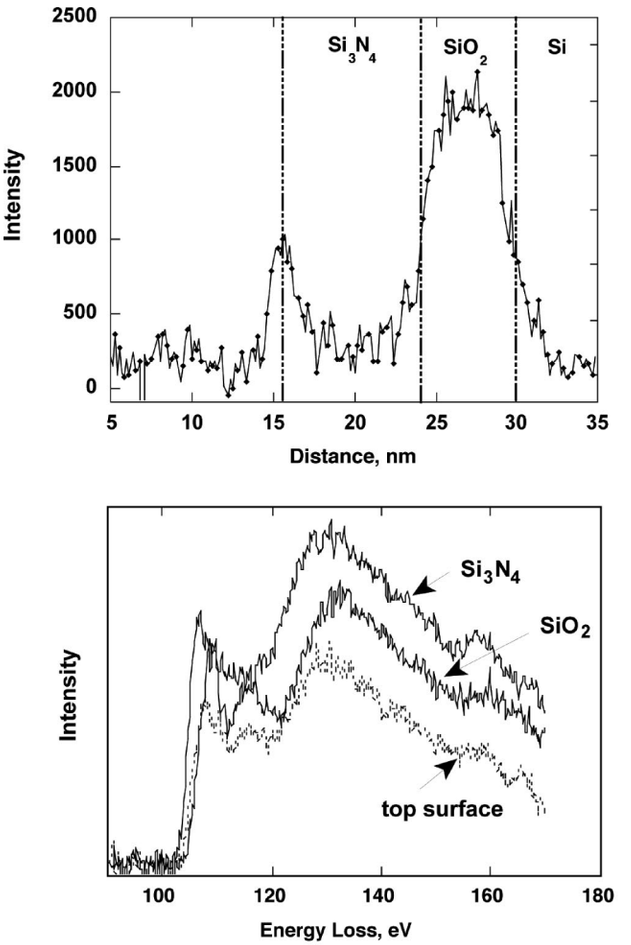


**Figure 3.** (a) Profile of the O-K integrated intensity across the ON stack. (b) Si-$L_{2,3}$ EELS profiles for the $SiO_2$ and $Si_3N_4$ layers, and the top surface of the ON stack. The shift of the Si-$L_{2,3}$ edge at the top surface is consistent with formation of the oxynitride. These data were recorded using GIF in a fixed-probe TEM.

that electron-beam irradiation of the nitride layer in the ONO stacks induced nitrogen segregation to the $Si/SiO_2$ interfaces;[8] the artifact occurred even at relatively low radiation doses. Subsequently, we developed a procedure for artifact-free EELS measurements of nitrogen profiles across the bottom $SiO_2/Si$ and the top $SiO_2$/poly-Si interfaces.[8] In this procedure, EELS spectrum images were recorded in a dedicated scanning TEM VG HB501 (100 kV, cold field-emission source) equipped with an Enfina EELS system (Gatan, Inc.), which incorporates a charge-coupled device (CCD) detector. The specimen was cooled down to liquid nitrogen temperature to prevent contamination buildup. The electron probe (1-1.5 nm diam) was scanned over an area encompassing the ONO stack, and EELS spectra containing the Si-$L_{2,3}$, O-K, and N-K edges were recorded at each point (pixel); the pixel size was kept close to 1 nm. Scans originating in the Si substrate and poly-Si cap layer were used to probe the $Si/SiO_2$ and poly-$Si/SiO_2$ interfaces, respectively; for each scan a freshly irradiated area was used. EELS spectrum images were acquired using a probe current of ~0.1 nA and a dwell time of 0.1 s. The beam was scanned parallel to the interfaces, and the individual spectra in the spectrum images acquired were summed along the scan-line direction to ensure sufficient counting statistics. Specimen drift during the data collection was corrected automatically by using a cross-correlation routine. The spectra were further processed to remove the spectral background, and the intensity under each edge

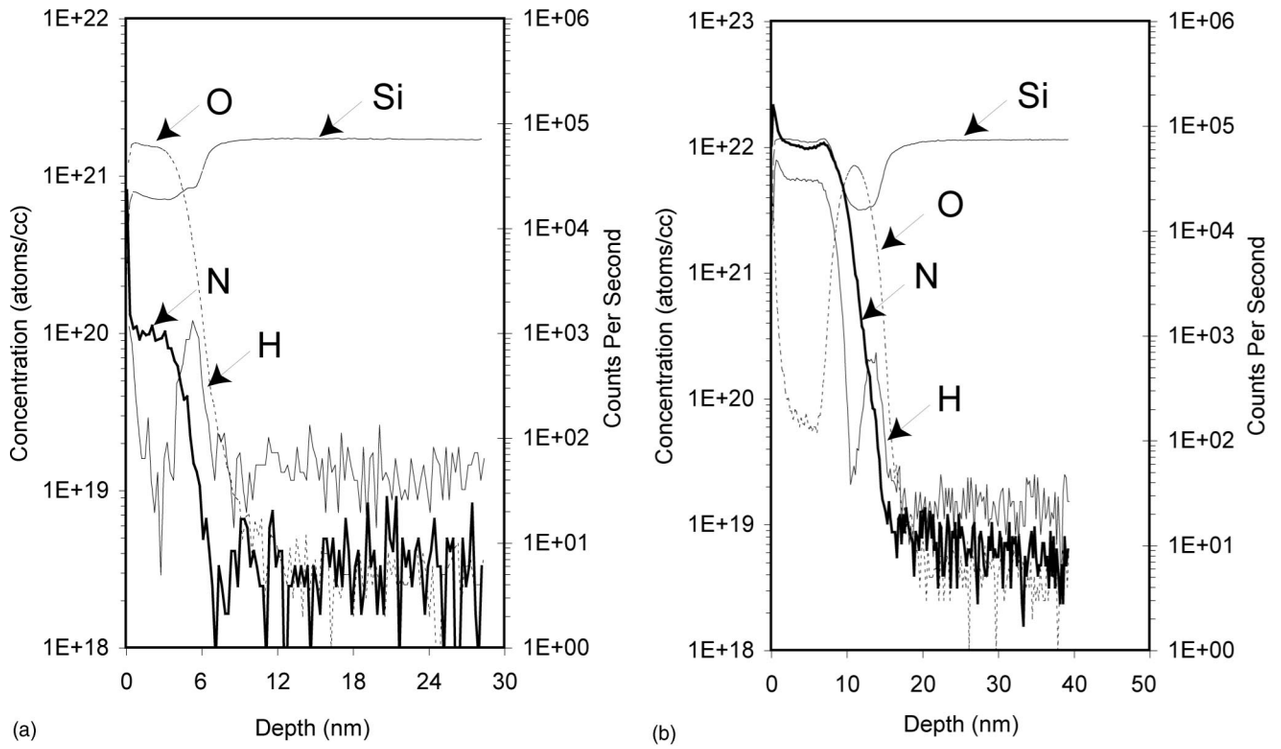


**Figure 4.** SIMS depth profiles of elemental distributions in the (a) BOX and (b) ON specimens. The contents of N and H were quantified using standards (left axis). The data for Si and O were not quantified and are presented in counts/s (right axis).

was integrated over a 10 eV energy window. Finally, the distributions of integrated intensities were obtained as a function of spatial coordinate.

SIMS measurements were conducted in a Physical Electronics ADEPT 1010 quadrupole SIMS instrument. The spectra were acquired using the Cs + 1 keV primary ion beam at 60° to the surface normal; the primary ion-beam energy and incident angle were chosen to optimize the depth resolution of the analysis. The H and N concentrations were quantified using silicon oxynitride (SiON) standards [characterized using nuclear reaction analysis (NRA)] and verified for accuracy with the use of a standardized control sample. Detection limits for N and H were estimated to be $4 \times 10^{18}$ and $2 \times 10^{19}$ atoms/cm$^3$, respectively. The spatial scale in the SIMS depth profiles was normalized to the total thickness of the corresponding films, as measured by XRR. Measurements on the ONO stacks with and without a poly-Si cap layer yielded identical results.

Electrical characterization of ONO-based memory cells was conducted using the *micro*Flash memory transistors (Tower Semiconductor, Ltd., Migdal Haemek, Israel) and metal-oxide semiconductor (MOS)-type capacitors with poly-Si electrodes. The *micro*Flash memory devices feature[2,11] 2 bits per SONOS transistor, where the local charge trapping occurs in the nitride layer of ONO. The memory cell is programmed using the channel hot electrons, while the erasing is accomplished by injecting holes generated by the band-to-band tunneling. Transistors based on the three types of ONO stacks (ONO-S, ONO-L, and ONO-TEOS, see Table I) were analyzed. Each transistor represented an element of the crosswise-patterned memory array and featured an effective channel length $L = 0.30$ μm and channel width (word linewidth) $W = 0.35$ μm. The initial (before cycling) values of a threshold voltage, $Vt$, (drain current $Id = 1$ μA, and drain bias voltage $Vdd = 1.6$ V) were 1.42 V (ONO-S), 1.85 V (ONO-L), and 1.58 V (ONO-TEOS), respectively. The difference in the initial values of $Vt$ for ONO-S and ONO-L stacks was associated with the different thickness of the top oxide. In contrast, lower $Vt$ for ONO-TEOS was attributed to the reduced density of negative (''chemical'') charge trapped in the top oxide layer of this stack.[12] The size of the memory window, defined as the difference between the values of $Vt$ in the programmed and the erased states, was 1.5 V. The memory transistors were subjected to endurance/retention test consisting of 10,000 program/erase cycles followed by a bake for 1 h at 250°C. The difference in the $Vt$ values before and after bake (closure of the memory window) was used as a measure of the device quality.

## Results and Discussion

*Compositional profiles.—EELS.*—A typical HRTEM image of the ONO stack (Fig. 1) reveals well-defined oxide (bright) and nitride (dark) layers. EELS measurements for both ONO-L and ONO-TEOS specimens yielded similar profiles of O-K and N-K characteristic intensity distributions (Fig. 2). Artifact-free measurements revealed no detectable nitrogen segregation to either bottom $SiO_2$/Si (Fig. 2a) or top $SiO_2$/Si (Fig. 2b) interfaces; the detection limit for nitrogen was estimated to be about 1-2 atom %. (Note that the radiation-induced segregation of nitrogen to the same interfaces was readily detectable.) The O-K intensity typically decreased to a noise level (2-3 atom %, 3σ) in the middle of the nitride layer (Fig. 2b). Occasionally, somewhat larger O-K intensity in the nitride (Fig. 2a) layer was observed and attributed to the beam-induced oxygen/nitrogen diffusion.[8] Existence of such beam-induced diffusion precluded reliable assessment of oxygen profiles in the nitride layers of the ONO stacks.

For the ON specimen, the presence of oxygen was detected in the thin surface layer (Fig. 3a), which indicates oxidation of the nitride surface upon exposure to air.[13,14] The energy of the Si-$L_{2,3}$ edge for the oxidized nitride surface is higher (by about 1 eV) than that for the underlying nitride layer (Fig. 3b), consistent with formation of a silicon oxynitride at the surface. This oxidized layer presumably remained at the interface between the nitride and the top oxide layers in the final ONO stacks, especially those with a TEOS-deposited top oxide. Apparent oxidation of the nitride surface correlates with

**Table II. Surface concentrations (atoms/cm$^2$) of N and H. The H1, H2, and H3 correspond to the top $SiO_2$/poly-Si interface, the nitride layer, and the bottom $SiO_2$/Si interface, respectively.[a]**

| Sample | N | H1 | H2 | H3 |
|---|---|---|---|---|
| BOX | $5.2 \times 10^{13}$ | — | — | $3.7 \times 10^{13}$ |
| ON | $1.1 \times 10^{16}$ | — | $4.9 \times 10^{15}$ | $9.0 \times 10^{13}$ |
| ONO-S | $1.0 \times 10^{16}$ | $2.8 \times 10^{14}$ | $7.0 \times 10^{14}$ | $3.0 \times 10^{13}$ |
| ONO-L | $1.0 \times 10^{16}$ | $4.9 \times 10^{14}$ | $7.2 \times 10^{14}$ | $2.2 \times 10^{13}$ |
| ONO-TEOS | $0.8 \times 10^{16}$ | $2.4 \times 10^{15}$ | $7.8 \times 10^{14}$ | $3.7 \times 10^{13}$ |

[a] The statistical uncertainties ($2\sigma$) are about 20%.

relatively poor reproducibility of electrical properties for the ONO-TEOS capacitors (see the following), where the extent of oxidation could control the electrical performance.

*SIMS*.—SIMS measurements on the single-layer thermal bottom oxide (Fig. 4a) revealed a low concentration of nitrogen (surface density $5.2 \times 10^{13}$ atoms/cm$^2$, Table II) uniformly incorporated in the layer. The incorporation of N into the oxide layer apparently occurred from the $N_2$ gas, which was pumped through the chamber during the thermal oxidation ($T = 900°C$).[15] Additionally, the thermal oxide contained $3.7 \times 10^{13}$ atoms/cm$^2$ of hydrogen at the $SiO_2$/Si interface. The hydrogen concentration at the $SiO_2$/Si interface increased further to $9.0 \times 10^{13}$ upon subsequent deposition of the nitride layer (Fig. 4b, Table III); the nitride layer contained $4.9 \times 10^{15}$ atoms/cm$^2$ of hydrogen. The nitrogen content in the oxide layer of the ON stack was difficult to ascertain because of the potential trailing of the nitrogen signal into the oxide; still, no clear segregation of the nitrogen to the $SiO_2$/Si interface was observed, consistent with the EELS measurements.

The hydrogen profiles for the complete ONO stacks featured three well-resolved maxima (Fig. 5, Table II), corresponding to the top $SiO_2$/poly-Si interface (H1), the nitride layer (H2), and the bottom $SiO_2$/Si interface (H3), respectively. The surface density of hydrogen at the $SiO_2$/Si interface, H1, decreased progressively on going from ONO-TEOS to ONO-S to ONO-L; that is, the hydrogen content at the Si/$SiO_2$ interface diminished with increasing thermal budget used to form the top oxide. The hydrogen content in the nitride layer (H2) also decreased considerably during growth/deposition of the top oxide from $4.9 \times 10^{15}$ atoms/cm$^2$ for the ON to $(7\text{-}7.8) \times 10^{14}$ atoms/cm$^2$ for the ONO stacks; however, all three ONO stacks exhibit similar concentration of hydrogen in the nitride. This evolution of hydrogen content in the nitride layers is attributed to the breaking of Si-H bonds at temperatures above 500-600°C upon growth of the top oxide, while the majority of the N-H bonds, which are stable up to significantly higher temperatures (>1000°C), remain intact.[16]

The SIMS nitrogen depth profiles for the ONO stacks revealed small (<1 atom/%) amounts of nitrogen incorporated into the top oxide layers; these concentrations were below the detection limits of the present EELS measurements. ONO-TEOS featured uniform distribution of nitrogen in the top oxide with a sharp top $SiO_2$/$Si_3N_4$ interface, as evidenced by the well-defined plateau in the corresponding nitrogen profile. In contrast, both ONO-S and ONO-L stacks exhibited a much broader distribution of nitrogen across the top oxide/nitride interface, which is consistent with the top oxide grown by nitride reoxidation. Present SIMS data do not provide conclusive evidence on the exact distribution and the amounts of nitrogen in the bottom oxide layers of ONO stacks; unfortunately, back-side SIMS measurements which could resolve these issues were not available for this study.

*XRR measurements*.—Both the density and thickness of individual layers in the three ONO specimens as measured by XRR (Fig. 6) are summarized in Table III. The statistical uncertainties ($2\sigma$) for the thickness and density measurements were about 1%. The XRR-derived thickness values agreed well with those measured from the HRTEM images; the scale in the HRTEM images was calibrated using {111} lattice fringes of Si. The three ONO specimens exhibited similar densities for the bottom oxide (2.18 g/cm$^3$), which were significantly larger than those of the top oxide layers in both ONO-S and ONO-TEOS specimens. In contrast, the density of the top oxide in the ONO-L specimen was comparable to that of the bottom oxide. The results suggest that longer reoxidation of the nitride increases the density of the resulting top oxide. The nitride layers in the three specimens exhibited similar densities of about 2.77 g/cm$^3$. XRR measurements for the single thermal oxide layer prior to nitride deposition yielded an average density of 2.11 g/cm$^3$, which was significantly lower than the 2.18 g/cm$^3$ deduced for the bottom oxide in the ONO stacks. Furthermore, fitting to the experimental XRR data suggested a significant density gradient in the single thermal oxide layer (BOX), with the density varying from 2.22 g/cm$^3$ for the bottom third of the layer to 1.99 g/cm$^3$ for the top third. These results suggest densification of the upper part of the bottom oxide layer upon subsequent deposition/growth of the nitride and the top oxide layers; similar results were reported by Santucci *et al.*[1] Such densification can be attributed, at least partly, to the incorporation of small amounts of nitrogen into the upper part of the bottom oxide layer. According to XRR, the oxide layers in the ONO stacks exhibited uniform densities, indicating that the XRR measurements were rather insensitive to the broad nitrogen distributions in the top oxide layers of the ONO-L and ONO-S specimens.

*Electrical characterization*.—The memory transistors built with all three ONO stacks (ONO-L, ONO-S, and ONO-TEOS) featured overall high endurance/retention characteristics (Fig. 7). Yet the transistors based on ONO-L exhibited the lowest reduction of *Vt* in the programmed state (after cycling and bake), while those based on ONO-TEOS yielded the worst performance. Note that both ONO-L and ONO-TEOS stacks feature nearly identical thickness for the oxide layers.[g] Furthermore, because the ONO stacks were processed at the first stages of the device fabrication, the thermal budget used in the processing of ONO had no influence on either the channel length or the drain engineering of memory transistors. Therefore, the differences in the performance of devices based on the different

[g] In a separate study, we confirmed that different thickness of the nitride layer had no effect on the *Vt* degradation.

**Table III. Thickness (nm) and density (g/cm$^3$) of individual layers in ONO stacks. The statistical uncertainty in the thickness derived from the HRTEM images is estimated to be ±0.5 nm ($2\sigma$). The relative statistical uncertainties for the thickness and density measured by XRR are 1% ($2\sigma$).**

| | Bottom oxide | | | Nitride | | | Top oxide | | |
|---|---|---|---|---|---|---|---|---|---|
| | Thickness | | Density | Thickness | | Density | Thickness | | Density |
| Specimen | TEM | XRR | XRR | TEM | XRR | XRR | TEM | XRR | XRR |
| ONO-S | 5.8 | 6.4 | 2.18 | 6.4 | 6.6 | 2.76 | 9.1 | 8.7 | 2.04 |
| ONO-L | 6.0 | 6.4 | 2.18 | 7.8 | 8.2 | 2.80 | 12.5 | 12.4 | 2.16 |
| ONO-TEOS | 6.0 | 6.0 | 2.22 | 6.3 | 6.1 | 2.77 | 13.1 | 13.4 | 2.04 |

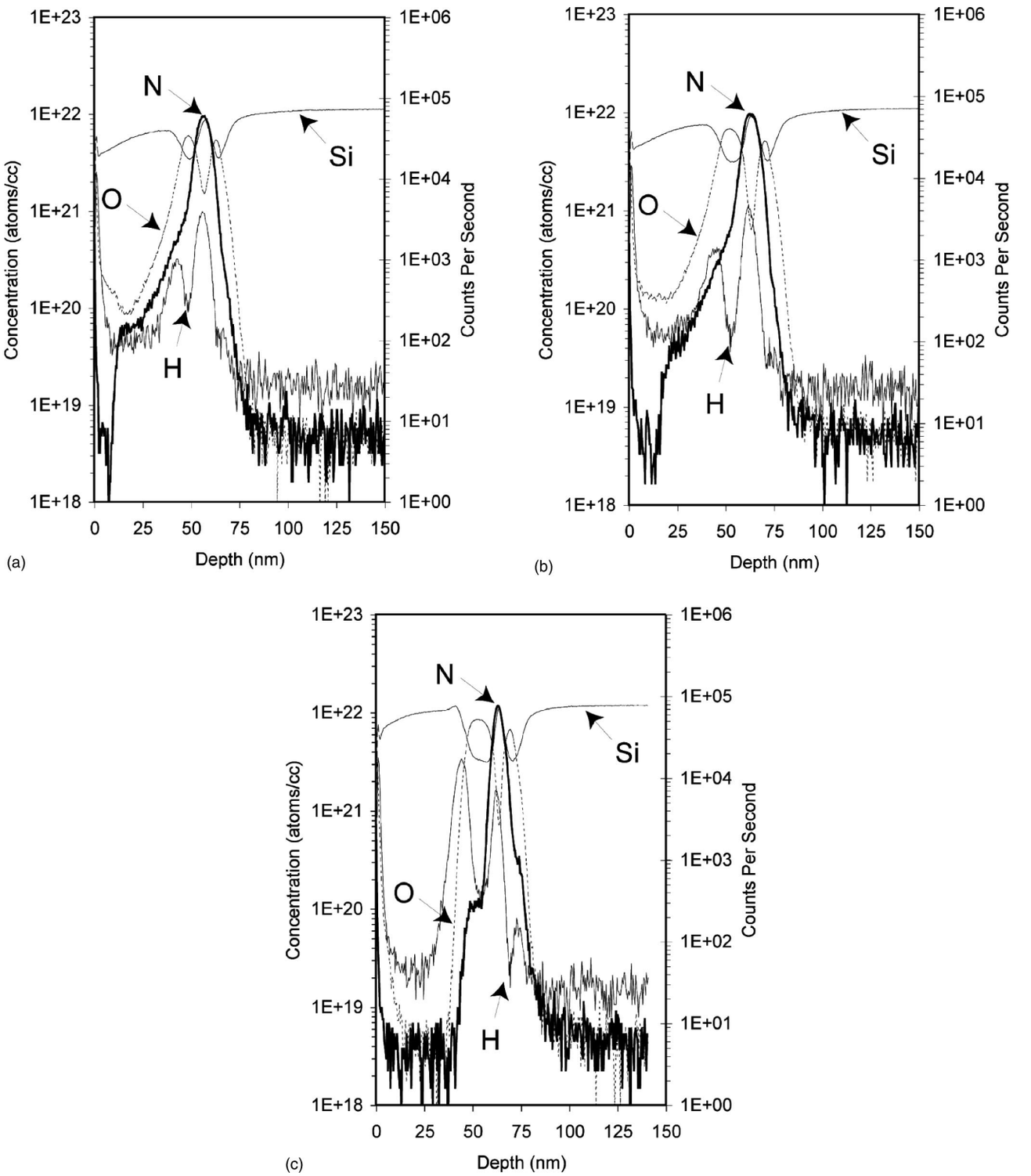


**Figure 5.** SIMS depth profiles of elemental distributions in the (a) ONO-S, (b) ONO-L, and (c) ONO-TEOS specimens. The contents of N and H were quantified using standards (left axis). The data for Si and O were not quantified and are presented in counts/s (right axis).

types of ONO are determined primarily by the structure and chemistry of individual layers and interfaces in these ONO stacks.

Compared to ONO-TEOS, both ONO-S and ONO-L stacks exhibit significantly broadened top $SiO_2/Si_3N_4$ interface, while ONO-L additionally features lower hydrogen content at the bottom $SiO_2$/Si interface, and higher density of the top oxide. Each of these factors is expected to improve the retention characteristics. In particular, the $SiO_2/Si_3N_4$ interfaces have been suggested to exhibit a high density of the electron and hole traps due to the presence of Si-Si bonds at the interface.[13] Thus, a broader top $SiO_2/Si_3N_4$ interfacial region is expected to yield better charge trapping characteristics. At the same time, lower concentration of hydrogen at the

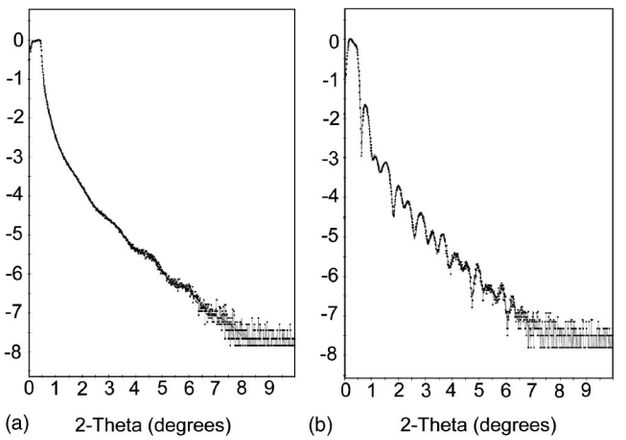


**Figure 6.** Experimental (dots) and calculated (lines) X-ray reflectivity profiles for (a) BOX (single-layer thermal oxide) and (b) ONO-L.

bottom $SiO_2$/Si interface is known to improve immunity to the hot carrier degradation.[18] Higher density of the top oxide, as observed in ONO-L, may suppress parasitic electron injection from a poly electrode during the erase procedure. At present, we cannot single out the dominant mechanism leading to the device improvement.

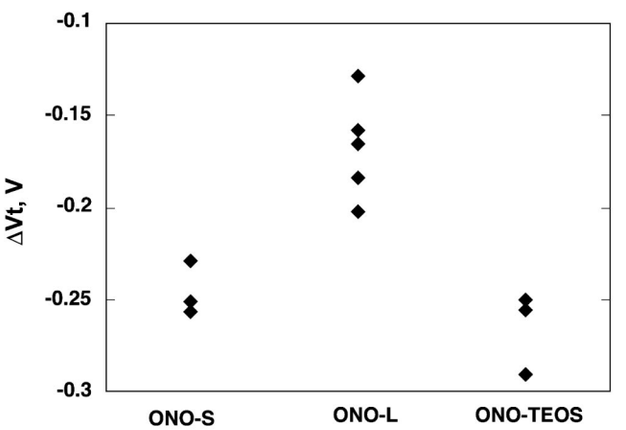


**Figure 7.** Reduction in the value of *Vt* for the SONOS 2-bit memory cell after bake at 250°C for 1 h followed by 10,000 program/erase cycles.

## Conclusions

The structure, chemistry, and electrical properties of ONO stacks with differently processed top oxide layers were compared. According to our results, using larger thermal budgets to fabricate the top oxide layer yields (*i*) lower amount of hydrogen at the bottom $SiO_2$/Si interface, (*ii*) broader distribution of nitrogen across the top oxide/nitride interface, (*iii*) higher density of the top oxide layer, and (*iv*) superior electrical performance in the resulting ONO-based memory transistors. Likely, each of the effects (*i*)-(*iii*) contributes to the improved electrical performance of the ONO-L stacks; however, the relative significance of each factor is difficult to determine. No nitrogen segregation to the $SiO_2$/Si interface was observed by EELS regardless of the thermal budget used to process the top oxide.

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## References

1. M. H. White, D. A. Adams, and J. Bu, *IEEE Circuits Devices Mag.*, **16**(4), 22 (2000).
2. E. Aloni, S. Kfir, M. Vofsy, and A. Ben-GuiGui, Pat. US 6,583,066 B2 (2003).
3. S. Santucci, L. Lozzi, L. Ottaviano, M. Passacantando, Picozzi, G. Moccia, R. Alfonsetti, A. Di Giacomo, and P. Fiorani, *J. Vac. Sci. Technol. A*, **15**, 905 (1997).
4. S. Santucci, L. Lozzi, M. Passacantando, A. R. Phani, E. Palumbo, G. Bracchitta, R. De Tommasis, A. Torsi, R. Alfonsetti, and G. Moccia, *J. Non-Cryst. Solids*, **245**, 224 (1999).
5. T. D. M. Saldago, C. Radtke, C. Krug, J. De Andrade, and I. J. R. Baumvol, *J. Electrochem. Soc.*, **146**, 3788 (1999).
6. Y. Ma, T. Yasuda, and G. Lucovsky, *Appl. Phys. Lett.*, **64**, 2226 (1994).
7. I. Banerjee and D. Kuzminov, *Appl. Phys. Lett.*, **62**, 1541 (1993).
8. I. Levin, R. D. Leapman, M. Kovler, and Ya. Roizin, *Appl. Phys. Lett.*, **83**, 1548 (2003).
9. T. Sasaki, K. Kuwazawa, K. Tanaka, J. Kato, and D.-L. Kwong, *IEEE Electron Device Lett.*, **24**, 150 (2003).
10. A. Halliyal, D. K. Foote, H. Komori, and K. W. Au, U.S. Pat. 6,248,628 (2001).
11. B. Eitan, U.S. Pat. 5,768,192 (1998).
12. Ya. Roizin, M. Gutman, S. Alfassy, and R. Yosefi, in *Proceeding of the NonVolatile Semiconductor Memory Workshop*, Monterey, CA, p. 83 (2003).
13. V. A. Gritsenko, H. Wong, J. B. Xu, R. M. Kwok, I. P. Petrenko, B. A. Zaitsev, Yu. N. Morokov, and Yu. N. Novikov, *J. Appl. Phys.*, **86**, 3234 (1999).
14. D. Landheer, P. Ma, W. N. Lennard, I. V. Mitchell, and C. McNorgan, *J. Vac. Sci. Technol. A*, **18**, 2503 (2000).
15. E. P. Gusev, H. C. Lu, T. Gustafsson, E. Garfunkel, M. L. Green, and D. Brasen, *J. Appl. Phys.*, **82**, 896 (1997).
16. F. de Brito Mota, J. F. Justo, and A. Fazzio, *J. Appl. Phys.*, **86**, 1843 (1999).
17. S. Santucci, A. V. la Cecilia, A. DiGiacomo, R. A. Phani, and L. Lozzi, *J. Non-Cryst. Solids*, **280**, 228 (2001).
18. T. Hore, H. Iwasaki, and K. Tsuji, *IEEE Trans. Electron Devices*, **36**, 340 (1989).